namely:

Vertex Detector Concepts & Technologies for an Apparatus at a Leptonic Collider

IAS program in High Energy Physics
HKUST Jockey Club
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1.BOUNDARY CONDITIONS:

what you shall keep in mind in mind while designing your Vertex Detector

✱ **PERFORMANCE**: primary & secondary vtx reconstruction starts by single tracks and the quality of the measured track is assessed by the perigee parameters, notably the **impact parameter (i.p.)**, namely the **distance of closest approach to the interaction point**. In the plane transverse to the beams, the resolution on the i.p. may be written as:

$$\sigma_{ip} = a \oplus \frac{b}{p \cdot \sin^{3/2}\theta}$$

- **a** depends on the single point resolution, the geometry (Inner & outer layer), the number of layers
- **b** depends on the Coulomb multiple scattering, i.e. the material budget in the beam pipe and the detector [dominated by the closer layer]

Past & future figures:

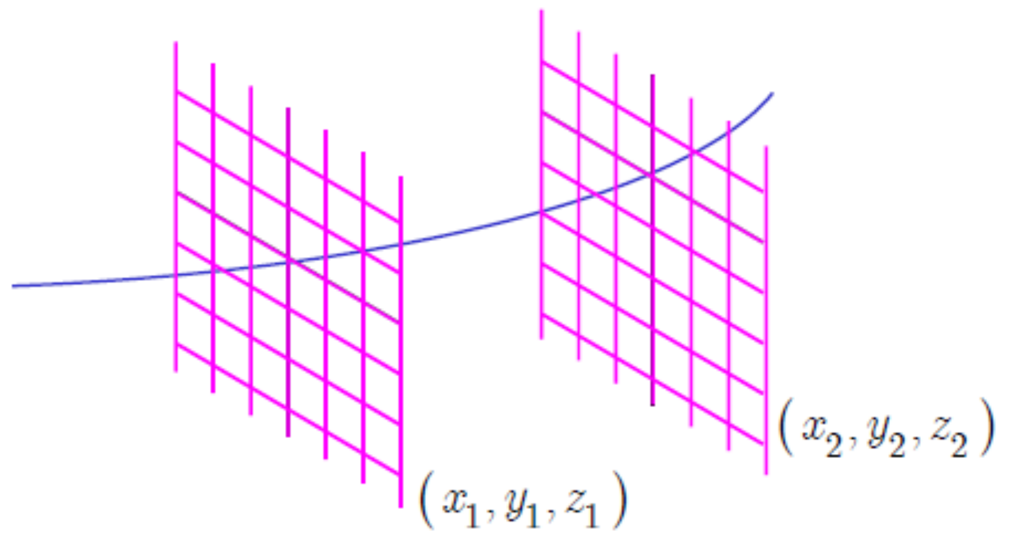
Accelerator	a [μm]	b [μm·GeV/c]
LEP	25	70
SLC	8	33
LHC	12	70
RHIC-II	13	19
ILC	< 5	< 10

ILD LOI 2009

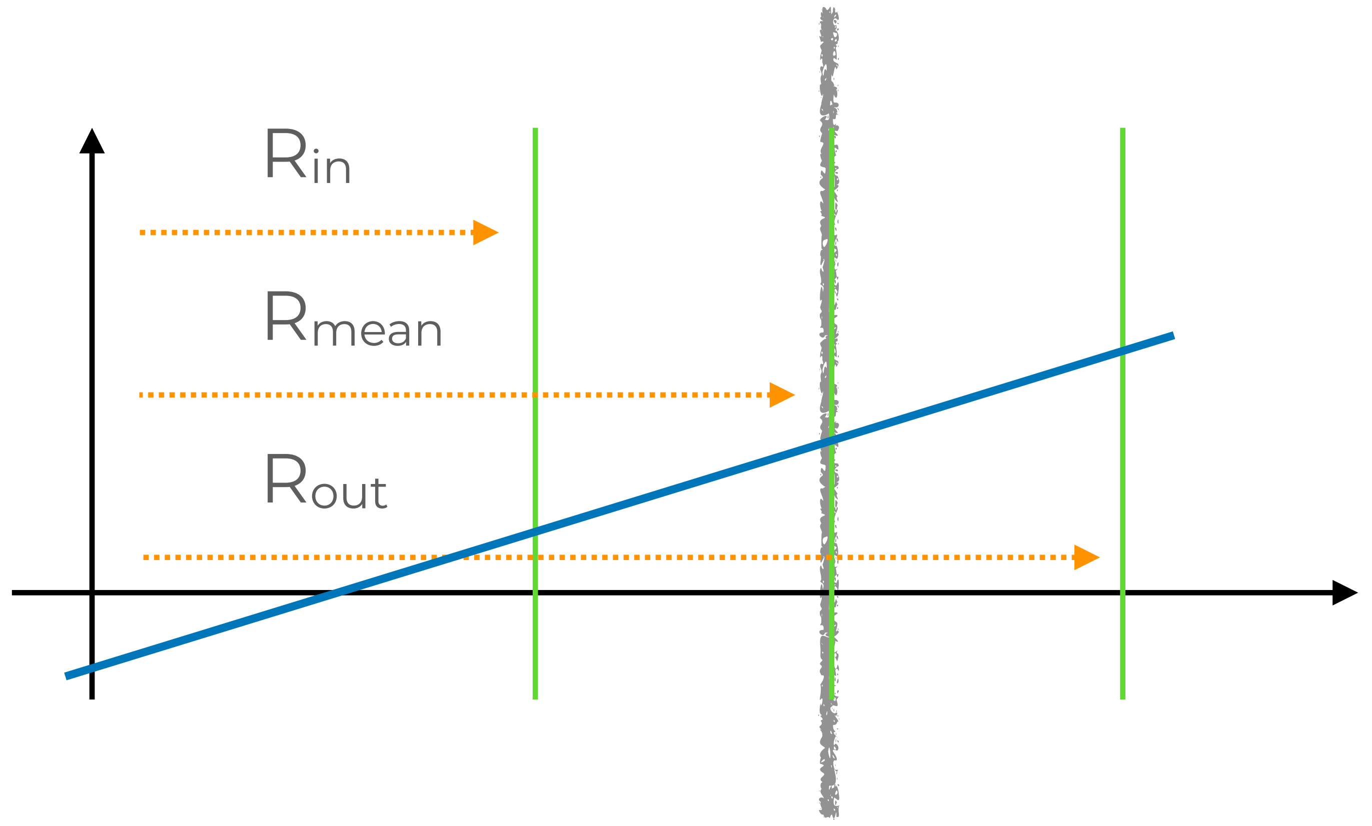
CEPC: **5** **10** CDR - 2018

N.B. initial values for LEP & LHC

1.Implications on the detector: asymptotic term, single point resolution & geomet



A simplified but possibly useful analytical model:



- R_{in} constrained by the beam pipe
- R_{out} loosely constrained by the surrounding detector
- no. layers n = 2m+1
- all of the detectors in the layers were born equal (same resolution)
- layers equally spaced
- the trajectory is a straight line
- the impact parameter is 1:1 geometrically correlated to the y value at R=0

Being so, the resolution may be analytically estimated as:

$$\sigma^2_{\tilde{y}} = \frac{\sigma^2_{single\,point}}{n} \times \left[1 + 12\frac{n-1}{n+1}\left(\frac{R_{mean}}{\Delta R}\right)^2\right] \quad = 25\ \mu m^2$$

R_{in} [mm]	R_{out} [mm]	n	$\sigma_{single\ point}$ [μm]
16	32.5	3	2.3
16	60.0	3	3.7
16	340	5	6.0
16	340	7	6.9

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16	60.0	3	3.7
16	340	5	6.0
16	340	7	6.9

If you are confident, as I was during my talk at HKUST in 2016, you can say that the vertex detector at the CEPC experiment is roughly like a Coke can:

If you get out a ruler, you'll find a standard Coke can is **12.2 cm** tall and the main body is **3.25 cm** in radius. It is difficult to accurately change the radius of our form, but we can make every other measurement use the default radius of 100 Imagine Units as a reference.

A Coke (TM) Can - Ian.Org
www.ian.org/d2i/FORMS.COKE.html

R_{in} [mm]	R_{out} [mm]	n	$\sigma_{single\ point}$ [μm]
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If you are a bit more conservative, on the detector side, you need a larger can:

The American can industry describes the dimensions of cylindrical cans by two three-digit numbers. The first number is the can's diameter and the second its height. In each number, the first digit is the number of whole inches, and the second two digits are the number of sixteenths of an inch. So, for example, a 303 by 407 can would be 3 03/16 inches in diameter and 4 07/16 inches high.

The table below lists some common can sizes.

Traditional name	Capacity in fluid oz.	Dimensions in inches	Can industry
202	4	2⅛ by 2⅞	202 by 214
Tall 202	5	2⅛ by 3½	202 by 308
8-Z short	7	2 11/16 by 3	211 by 300
No. 1	10	2 11/16 by 4	211 by 400
Tall no. 1	12	2 11/16 by 4 13/16	211 by 413
300	14	3 by 4 7/16	300 by 407
303	16	3 3/16 by 4⅜	303 by 406
Short no. 2	14	3 7/16 by 3⅜	307 by 306
No. 2	19	3 7/16 by 4 9/16	307 by 409
Tall no. 2	24	3 7/16 by 5 9/16	307 by 509
No. 2½	28	4 1/16 by 4 11/16	401 by 411
No. 3	32	4¼ by 4⅞	404 by 414
Tall no. 3	46	4¼ by 7	404 by 700
2 lb coffee	66	5⅛ by 6½	502 by 608
No. 10 (same as 3-lb coffee can)	105	6 3/16 by 7	603 by 700

https://www.sizes.com/home/cans.htm

but you still need to keep it cold! Or at least @ room T

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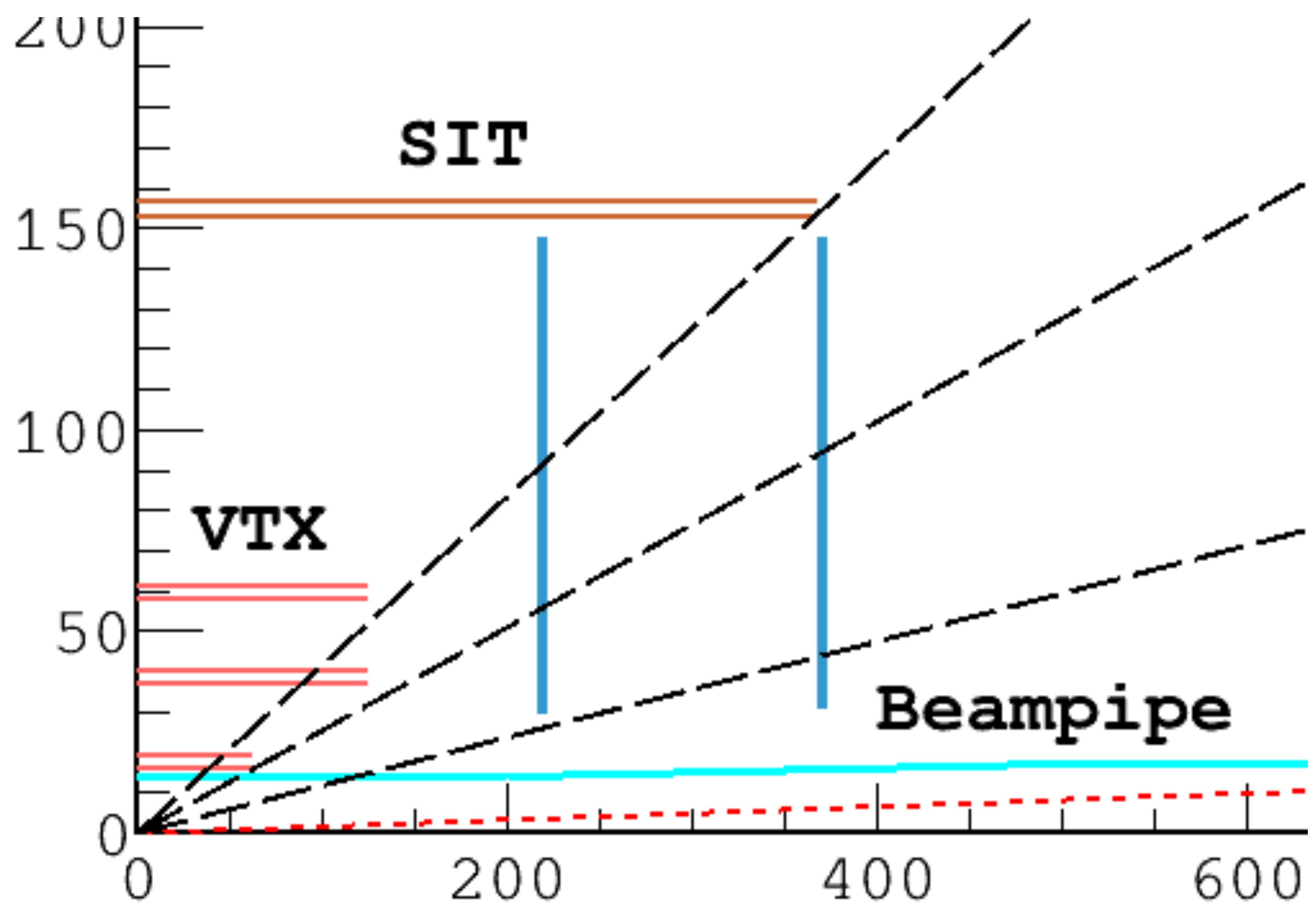


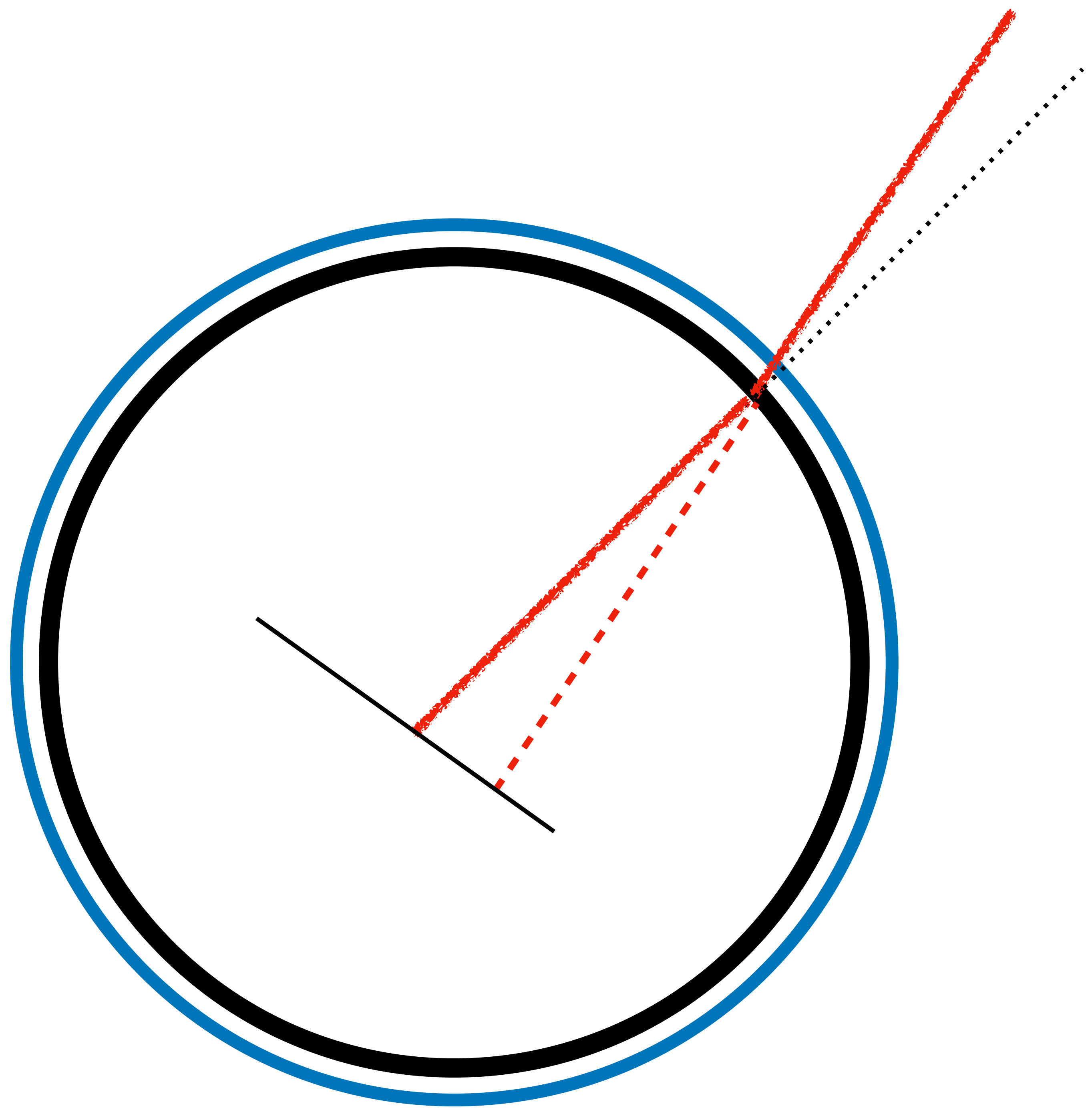
The CEPC-CDR baseline vertex detector geometry

	R (mm)	$\lvert z\rvert$ (mm)	$\lvert\cos\theta\rvert$
Layer 1	16	62.5	0.97
Layer 2	18	62.5	0.96
Layer 3	37	125.0	0.96
Layer 4	39	125.0	0.95
Layer 5	58	125.0	0.91
Layer 6	60	125.0	0.90

about 4” 1/4 **about 5”**

(do not forget wafers today are 8” in diameter)

2.Implications on the detector & beam pipe: multiple scattering term & material budget



Our event horizon is defined by the beam pipe and stochastic deviations in the particle direction due to multiple Coulomb scattering are irreducibly affecting our capability to measure the perigee parameters.
Following the Moliére's theory, the standard deviation of the Gaussian core of the angular deflection in the transverse plane can be written as:

$$\theta_0 = \frac{13.6 \text{ MeV}}{\beta c p} \, z \, \sqrt{x/X_0}\Big[1 + 0.038 \ln(x/X_0)\Big]$$

where x is the thickness, X_0 the radiation length and the effect on the impact parameter resolution, presuming to have no uncertainty on the "pivot point" at the beam pipe, is:

$$\sigma_{m.s.} = R_{beam\,pipe} \times \theta_0 = \frac{b}{p\,sin^{3/2}\theta}$$

where θ is the polar angle.

Estimates of the contributions due to the multiple scattering in the Berillium beam pipe & constraints on the VTX

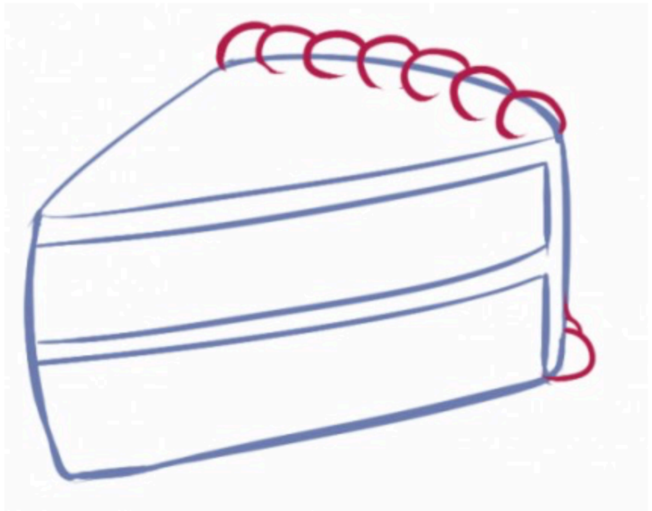
Machine/Exp.	R_{bp} [mm]	Thickness [mm]	x/X_0 [%]	$b_{beam\ pipe}$ [µm]
LEP/DELPHI	56	1.4	0.40	48
LHC/ATLAS	23.5	0.8	0.23	15
ILC/TESLA Det.	14	0.5	0.14	7
CEPC (CDR2018)	**15**	**0.5**	**0.14**	**8**

The inner layer of the VTX detector is adding a second scattering surface; being the deflections uncorrelated and summing up in quadrature the contributions, one can see that:

$$b \approx 10\mu m \rightarrow x_{VTX\ inner\ layer}/X_0 \leq 0.15\%$$

namely an effective thickness equivalent to 140 µm of Silicon, certainly NOT a piece of cake

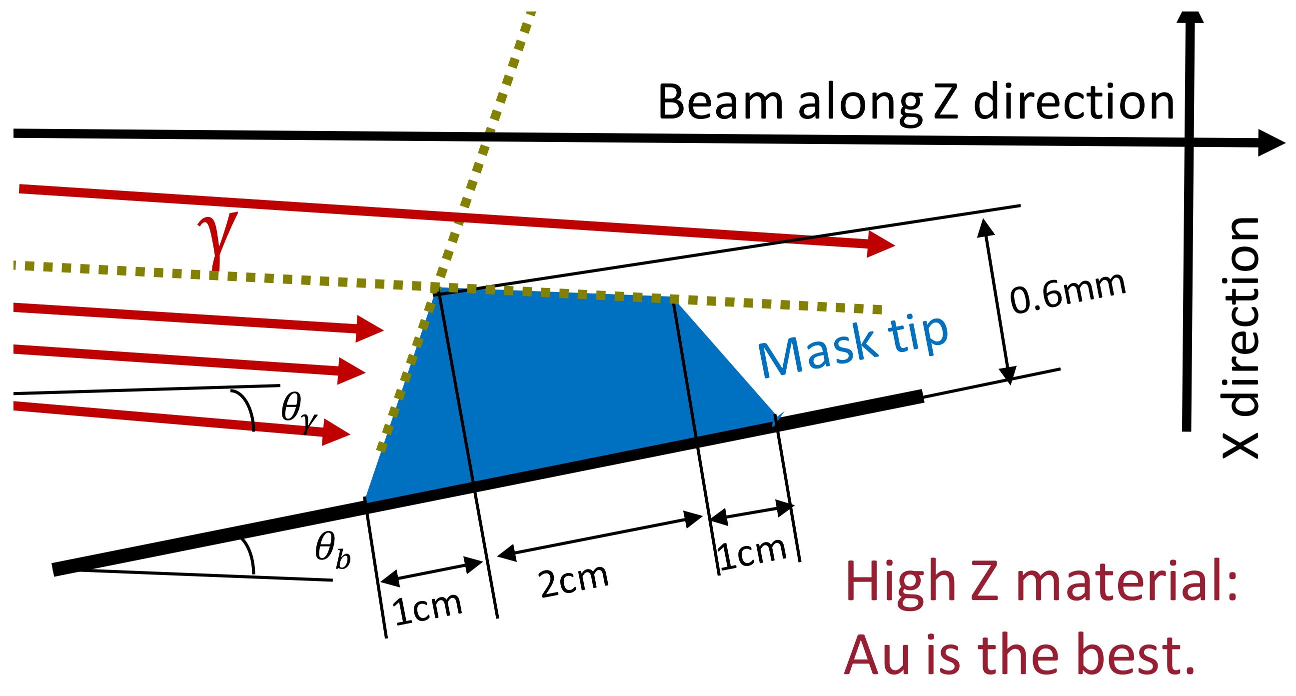
(well, not necessarily bad if you have to be THIN)

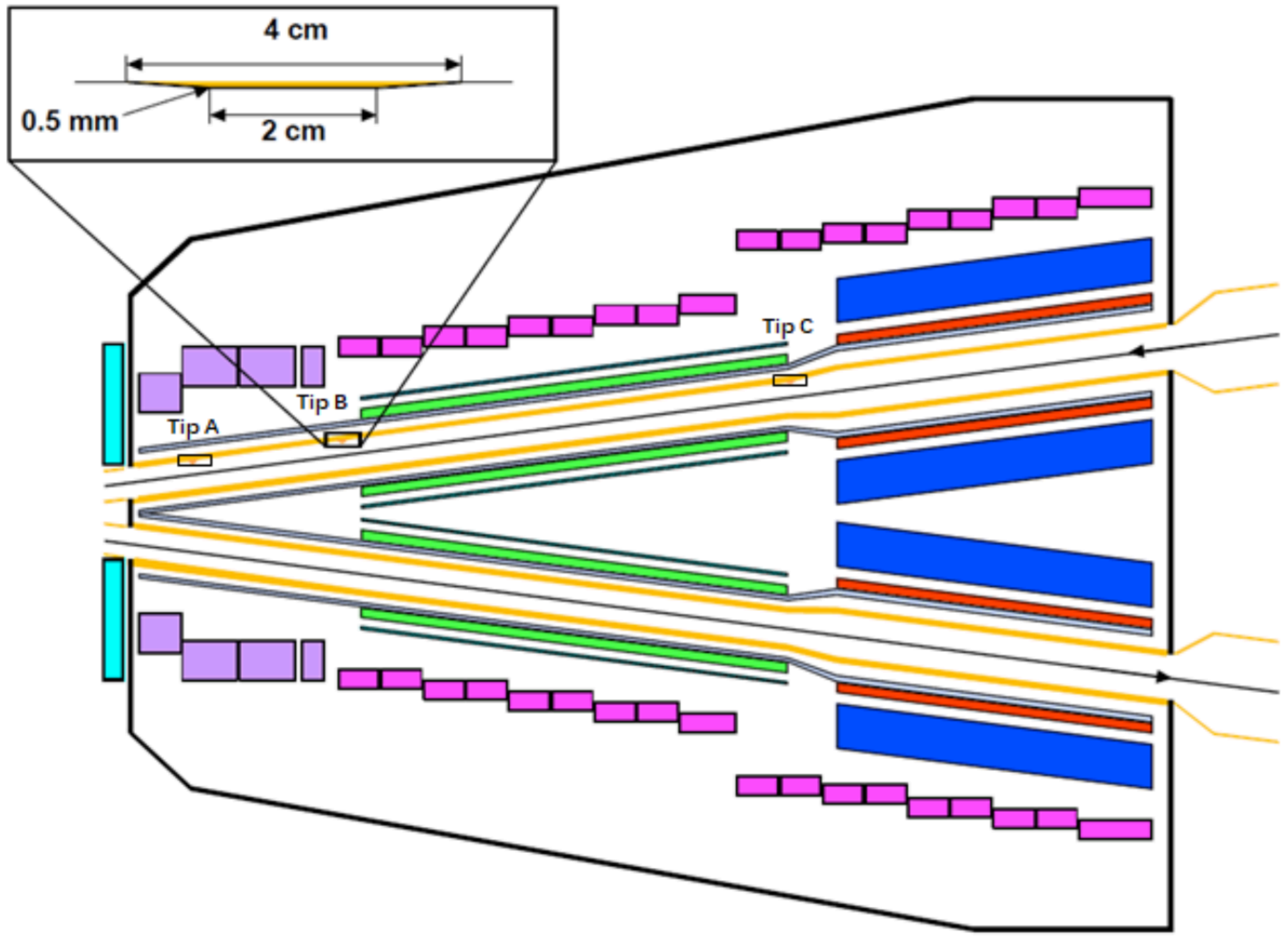


✱ BEAM INDUCED BACKGROUND at the CEPC*:

Synchrotron radiation photons from the last bending dipole magnet:

- it may be a killer once the photons scatter in the beam pipe and enter the detector region;
- mask tips are an effective therapy and reduce by nearly 3 orders of magnitude the number, from 40 000 to less than 80 photons hitting the beam pipe /beam crossing (BX) ⇒ **NEGLIGIBLE EFFECT**





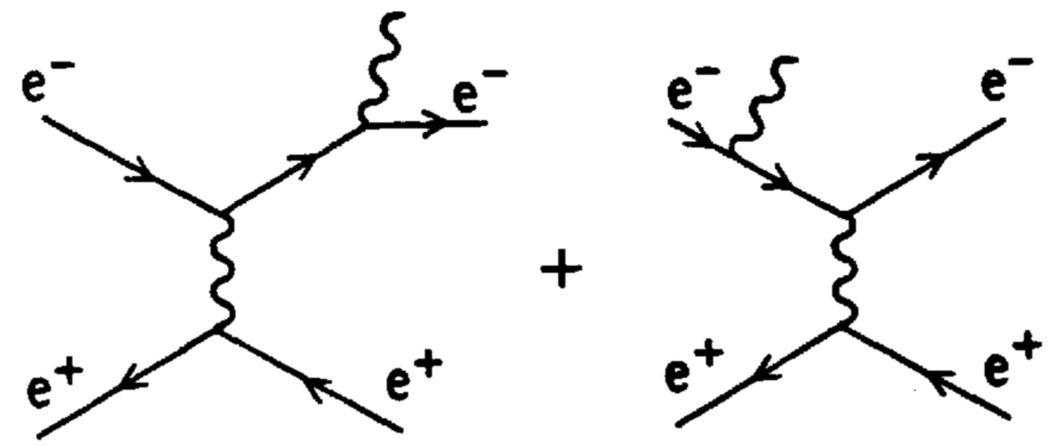
tips located at z = ±1.51, ±1.93, ±4.2 m

* based on the work coordinated by Hongbo Zhu, summarised in the CEPC-CDR + Report by Wei Xu at the Beijing 2017-11 workshop

✱ BEAM INDUCED BACKGROUND at the CEPC*:

Off-energy particles entering the interaction region:

- as long as beam particles loose more than 1.5% of their nominal energy, they cannot fit the “normal” orbit;
- energy loss is due to beam-gas interaction anywhere (residual pressure 10^{-7} mbar), beamstrahlung and radiative Bhabha [the DOMINANT effect] in the ip region;



+ s-channel diagrams

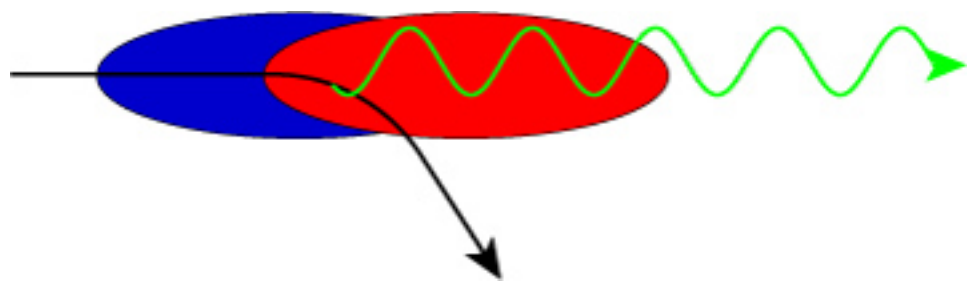
- stray particles can enter the detector volume right after the bunch crossing or after multiple turns;
- collimators are quite effective in reducing the effects due to off-energy particles:

  - APTX1, APTX2, horizontal plane, 5 mm aperture (14 σ_x)
  - APTY1, APTY2, vertical plane, 1 mm aperture (39 σ_y)) in the 1700 m < |z| < 2300 m region

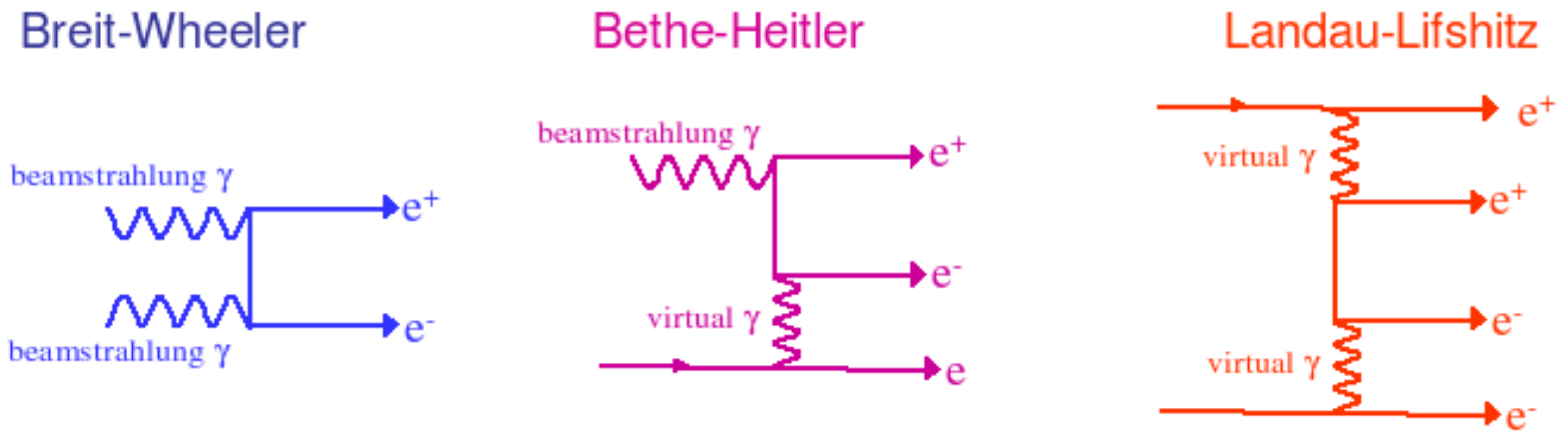
⇒ residual hit density at the inner layer of the VD: 0.22 hits/cm²/BX (safety factor 10; $\sqrt{s}$ = 240 GeV)

* based on the work coordinated by Hongbo Zhu, summarised in the CEPC-CDR + Report by Wei Xu at the Beijing 2017-11 workshop

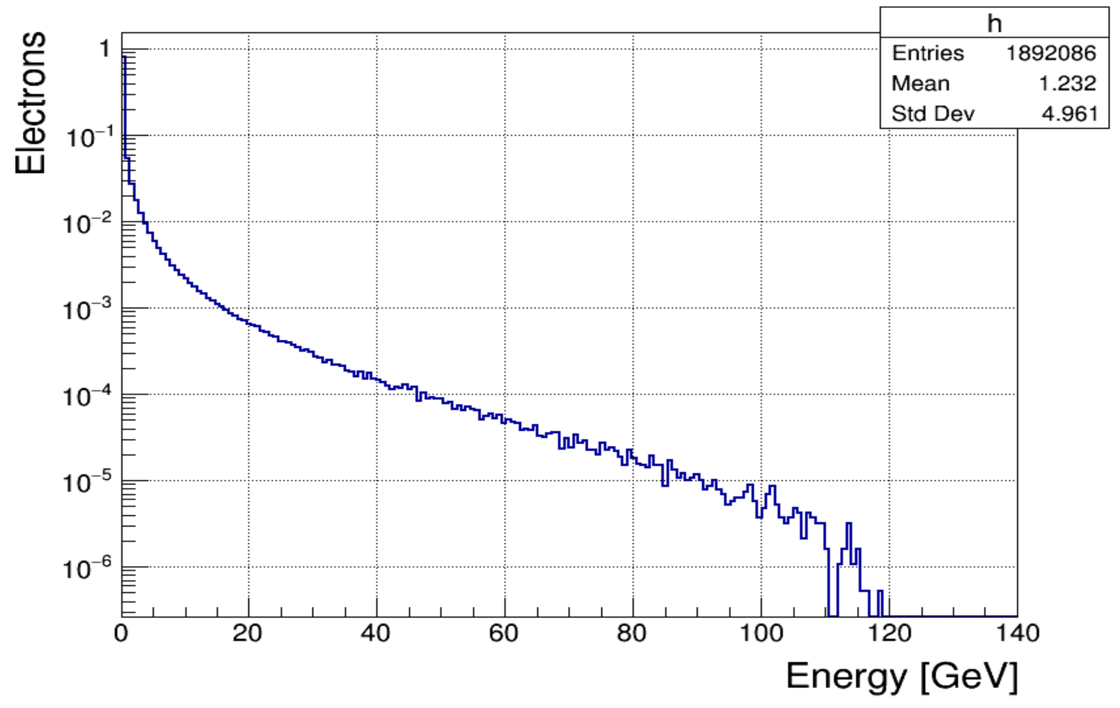
✱ BEAM INDUCED BACKGROUND at the CEPC*:

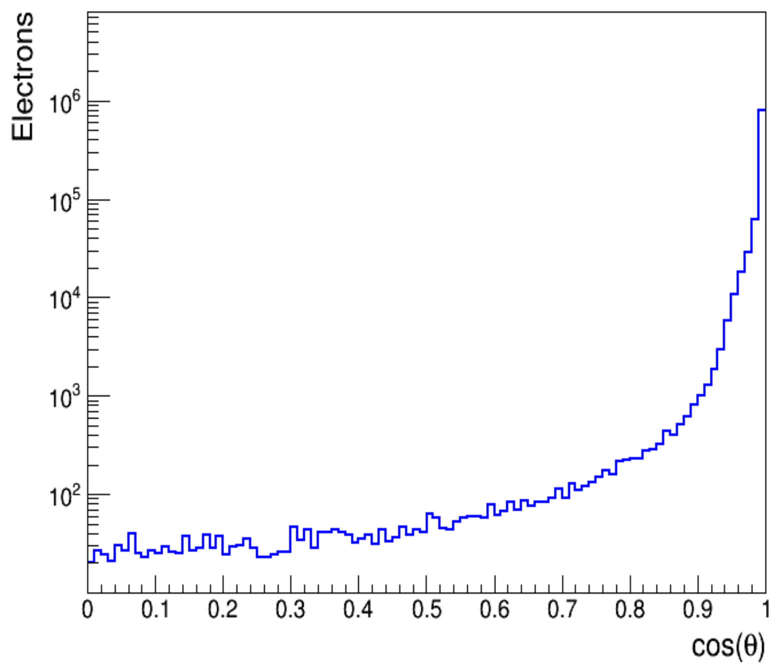


- **e+e- following a photon-photon interaction during the beam crossing: process :**



- the energy spectrum and the polar angle distribution are such that the majority (84% if I'm not mistaken, after Wei Xu) are confined within the beam pipe:





⇒ major source of background hits at the level of: 2.2 hits/cm²/BX @inner VD layer, decreasing by 2 orders of magnitude at the outer layer at 6 cm (safety factor 10 in the estimates; $\sqrt{s}$ = 240 GeV)

* based on the work coordinated by Hongbo Zhu, summarised in the CEPC-CDR + Report by Wei Xu at the Beijing 2017-11 workshop

✱ BEAM INDUCED BACKGROUND at the CEPC, summary table:

	H (240)	W (160)	Z (91)
Hit Density [hits/cm^2·BX]	2.4	2.3	0.25
TID [MRad/year]	0.93	2.9	3.4
NIEL [10^{12} 1 MeV n_{eq}/cm^2·year]	2.1	5.5	6.2

CEPC

by the way, this is what was estimated at the ILC*:

Layer	1	2	3	4	5	6
0.5 TeV	6.3±1.8	4.0±1.2	0.25±0.11	0.21±0.09	0.05±0.03	0.04±0.03
1 TeV	11.8±1.0	7.5±0.7	0.43±0.13	0.36±0.11	0.09±0.04	0.08±0.04

ILC-TDR

M. Winter, ALCW 2015;

what is the impact on the detector architecture? say that, for Pattern Recognition & efficiency,

⇒ you do not want to exceed 1% occupancy

*but beware of the fact numbers can be larger by a factor 2-3 in the ILC250 scheme, see Anne Schutz, arXiv:1801.04156, 2018

Once more, some back-of-an-envelope calculations:

say you have:

- **2.4 hits/cm^2/BX**
- **20x20 μm^2 pixels ⇒ 1/4 Megapixel/cm^2**
- **every hit, is generating a 3x3 pixel cluster ⇒ about 20 fired pixels/cm^2/BX**

⇒ targeting 1% occupancy, the maximum number of BX you can integrate is 125, namely

Δt = 85 μs for 1 cm^2 sensor

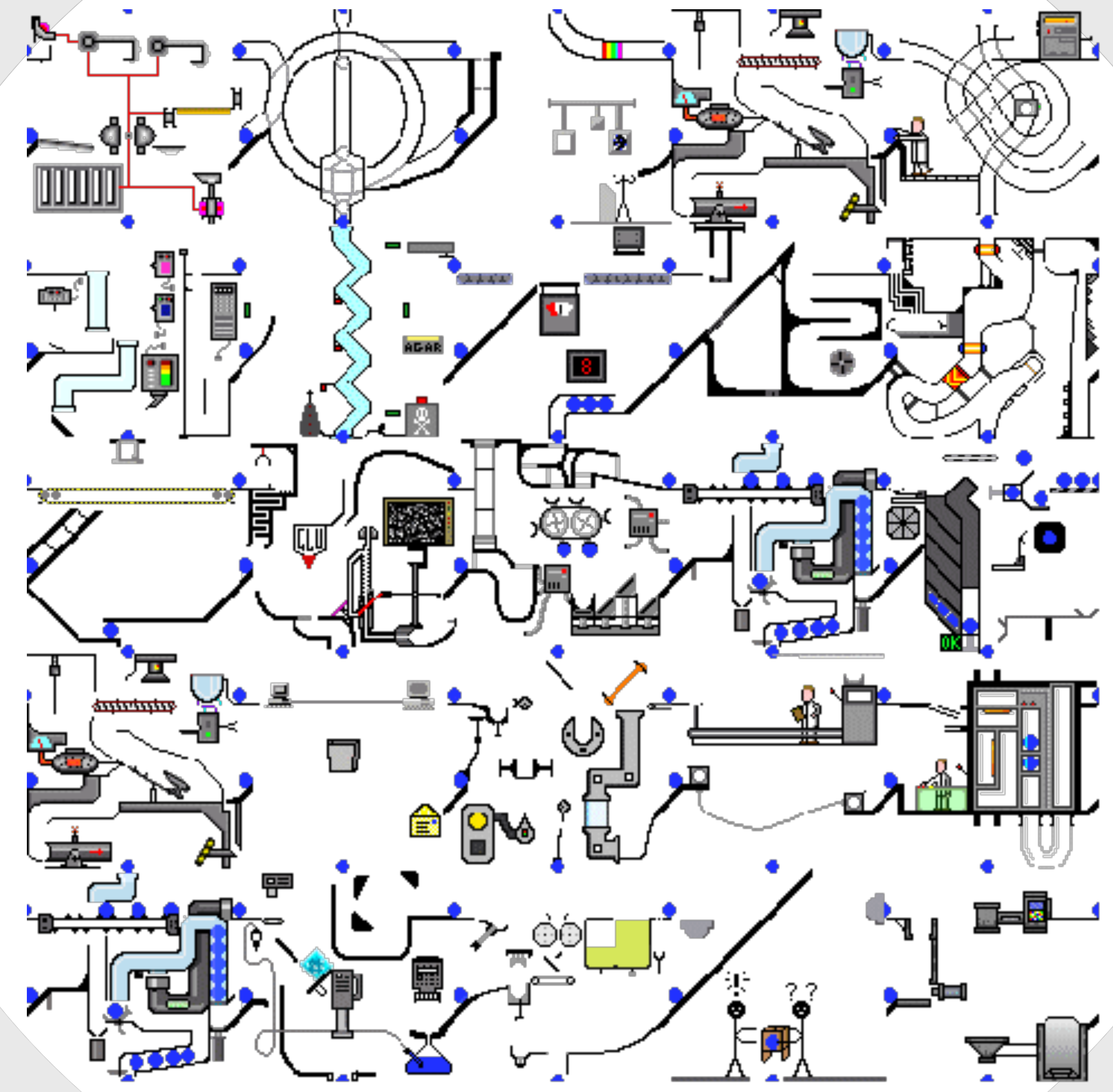
meaning that I either have

- ONE full frame read-out in less than 85 μs [independent from the no. of fired pixels]

or, in a data-driven (push) architecture,

- 2500 pixels (1% of the existing ones) addressed & read-out (effective read-out time ÷ no. fired pixels), namely 34 ns/pixel

no matter the architecture, you have to be FAST ⇒ “burn” energy ⇒ “grow in mass”



READY TO GO?

a glance at the state-of-the- art and beyond

2. MECHANICS & INTEGRATION

where SIZE & HEAT do matter

- Something BIG & LIQUID COOLED
- Something SMALLER & AIR COOLED
- Something NEW

Essential bibliography:

- Slides & thoughts from Corrado Gargiulo's Detector seminar @CERN, October 26, 2018
- The HKUST2019 report by Rafael Coelho Lopes de Sà on Recent Developments in Silicon tracker mechanics
- TDR of the ALICE Inner tracker J. Phys. G: Nucl. Part. Phys. **41** (2014) 087002 [comprehensive description]
- P. Martinengo, The new Inner Tracking System of the ALICE experiment, Nuclear Physics A 967 (2017) 900–903 [short & compact]
- G. Contin et al., The STAR MAPS-based PiXeL detector, arXiv 1710.02176v2, Jan. 22nd 2018
- F. Duarte Ramos et al., CLIC inner detectors cooling simulations, LCD-Note-2013-007
- N. Berger et al., A tracker for the Mu3e experiment based on high-voltage monolithic active pixel sensors, NIM A 732 (2013) 61–65 + reports @VTX conferences
- A. Numerotski et al., PLUME collaboration: Ultra-light ladders for linear collider vertex detector, NIMA 650 (2011) 208–212 & updates (see the slides at the LC detector workshop 2017)
- Reports by the DEPFET collaboration on the all-silicon module development, including:
    1. The CEPC Beijing 2018 workshop by Marcel Vos
    2. The HKUST2019 report by Laci Andricek
    3. L. Andricek et al., Integrated cooling channels in position-sensitive silicon detectors, JINST 11 (2016) no. 06, P06018

✱ Something BIG & LIQUID COOLED: the ALICE ITS (supposed to be installed in the 2019-2020 shutdown)

- based on binary monolithic active pixel sensors (ALPIDE), thinned to 50 μm
- pixel size: 29x27 μm^2
- TOTAL NUMBER OF PIXELS: 12.5 x 10^9 (30 000 chips)
- **CHIP Power consumption: 40 mW/cm^2**
- **TOTAL POWER: 5 kW**
- Operating temperature: 23C

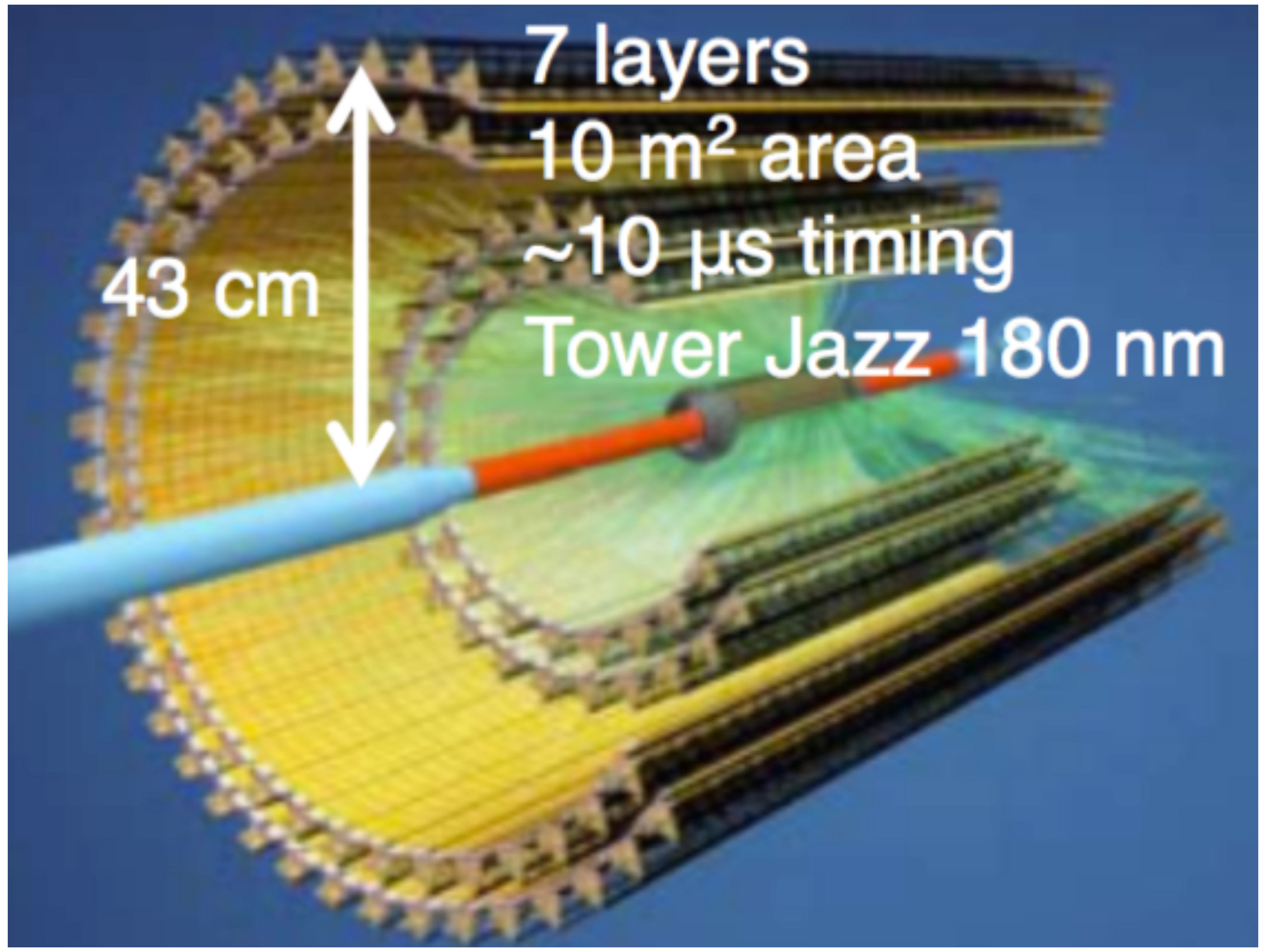
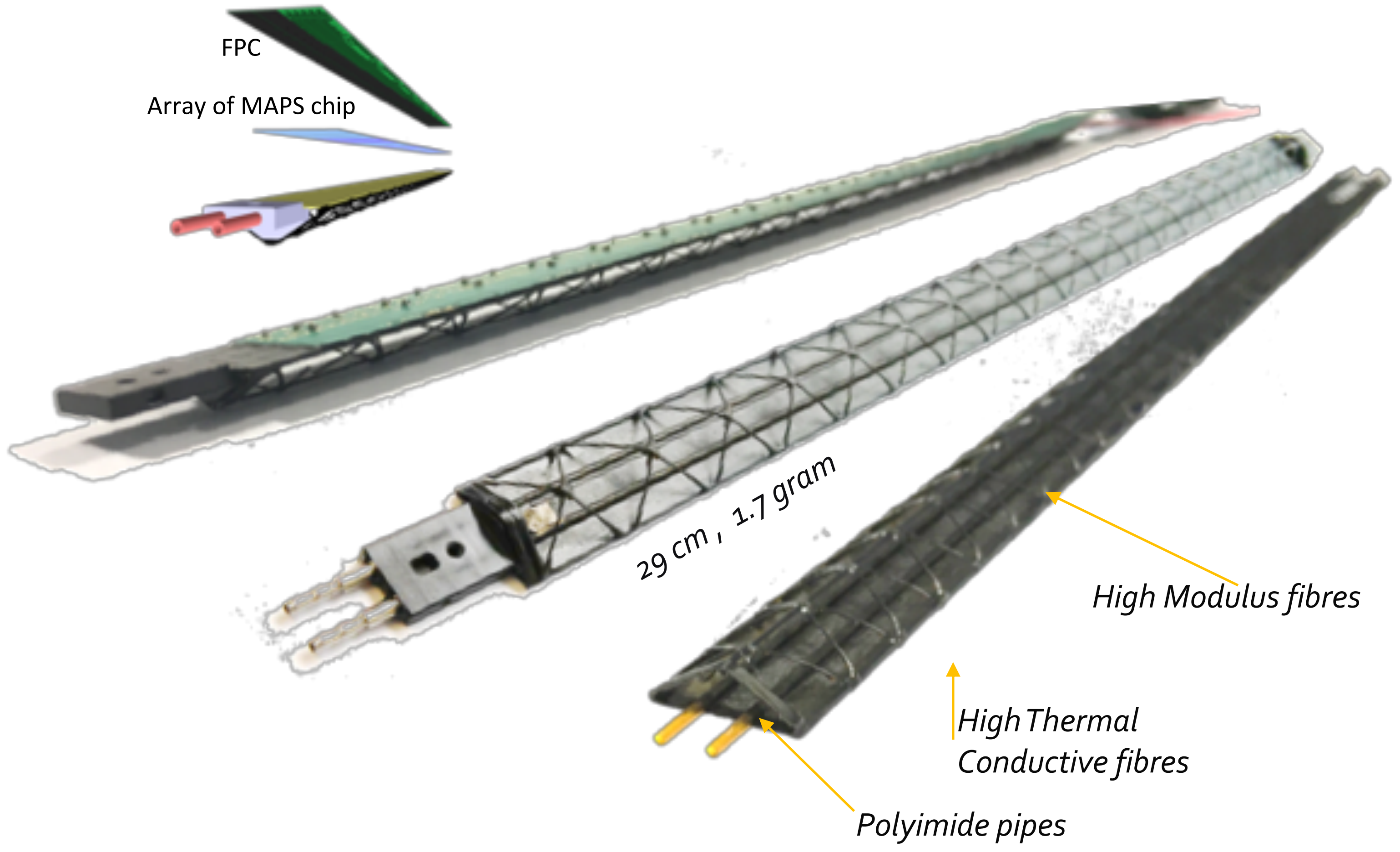
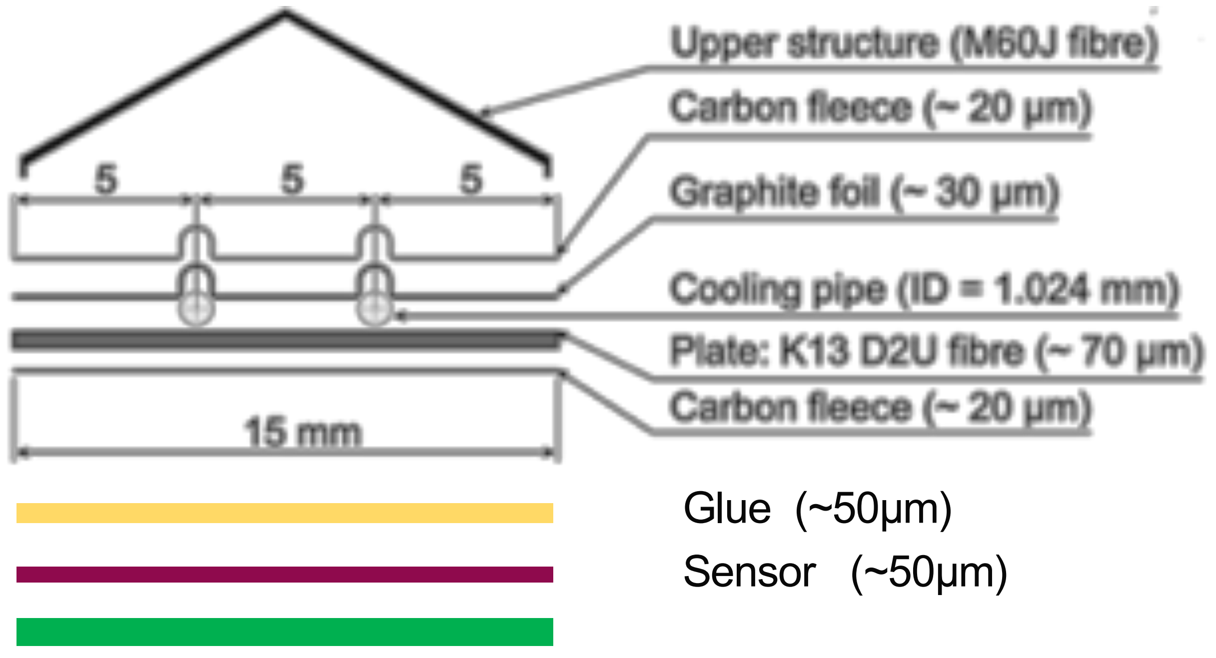
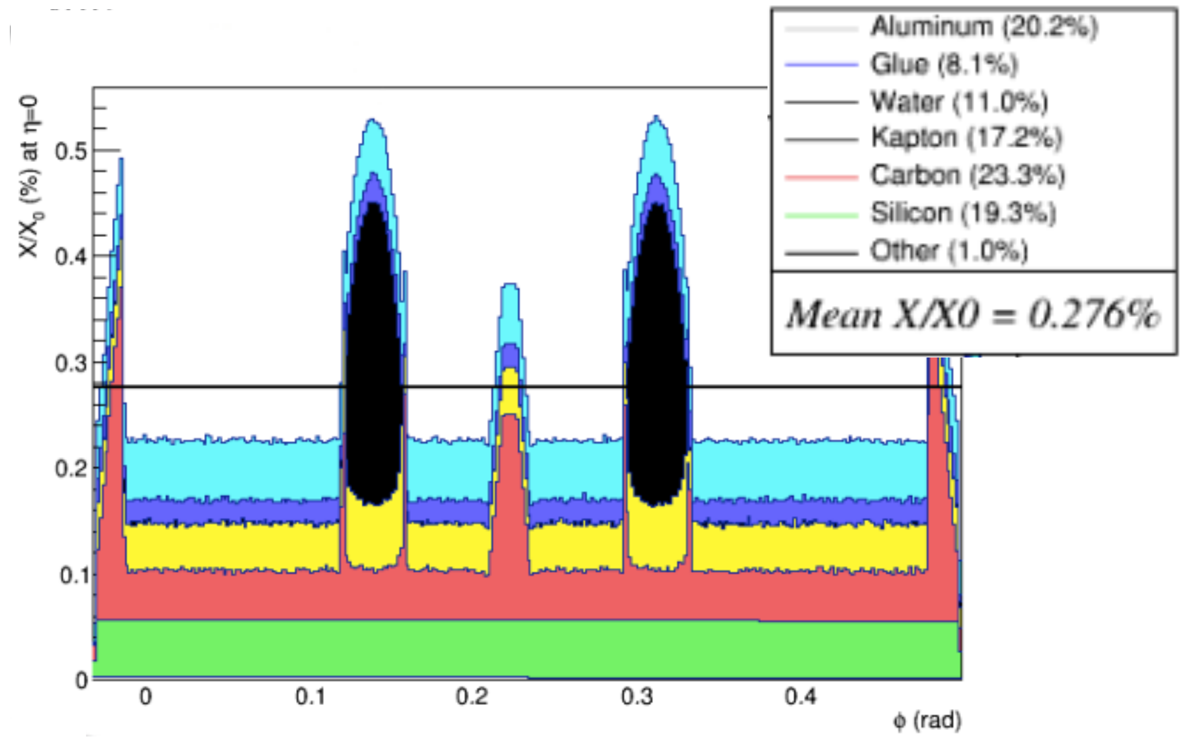


Table 1.1: Geometrical parameters of the upgraded ITS.

	Inner Barrel			Outer Barrel			
	Inner Layers			Middle Layers		Outer Layers	
	Layer 0	Layer 1	Layer 2	Layer 3	Layer 4	Layer 5	Layer 6
Radial position (min.) (mm)	22.4	30.1	37.8	194.4	243.9	342.3	391.8
Radial position (max.) (mm)	26.7	34.6	42.1	197.7	247.0	345.4	394.9
Length (sensitive area) (mm)	271	271	271	843	843	1475	1475



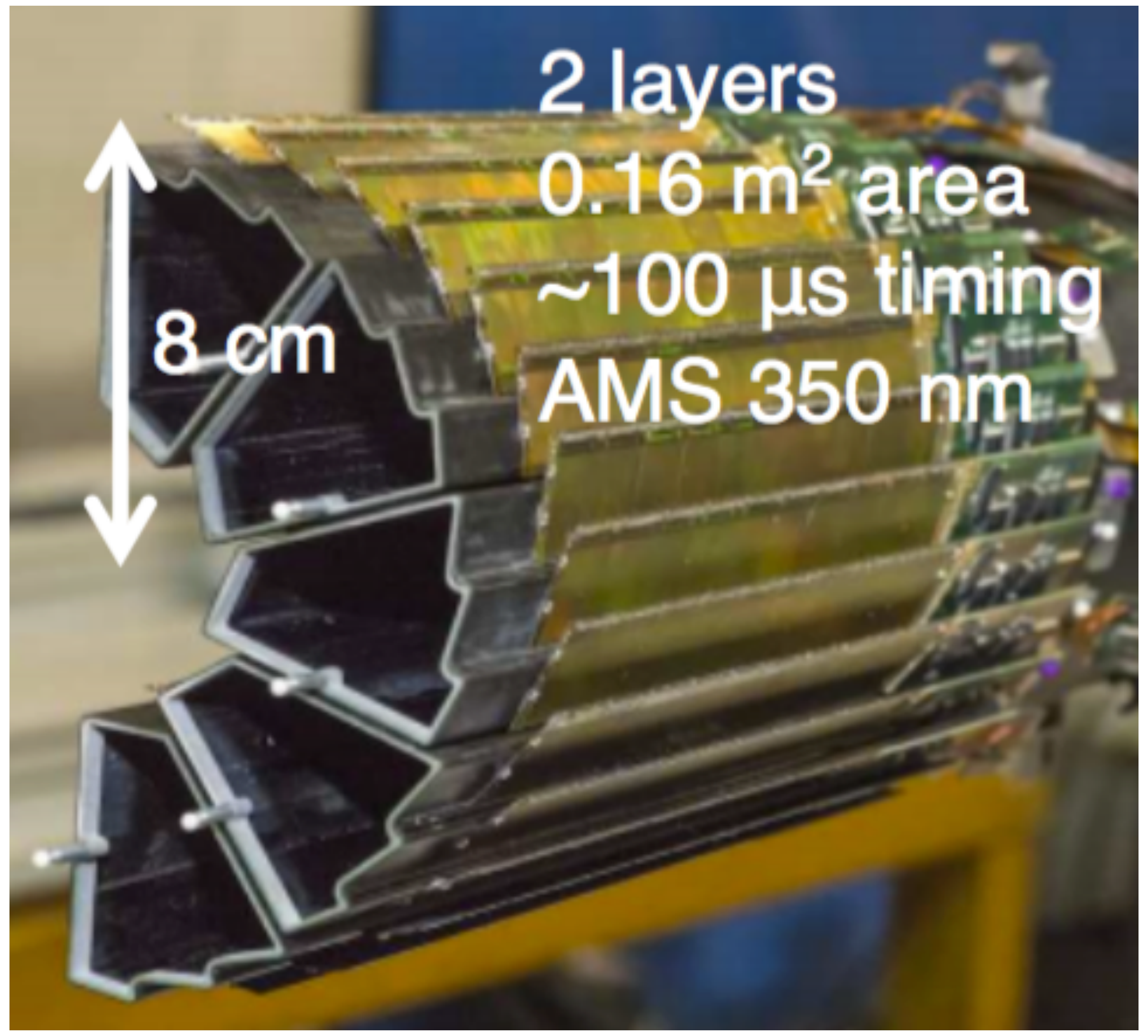


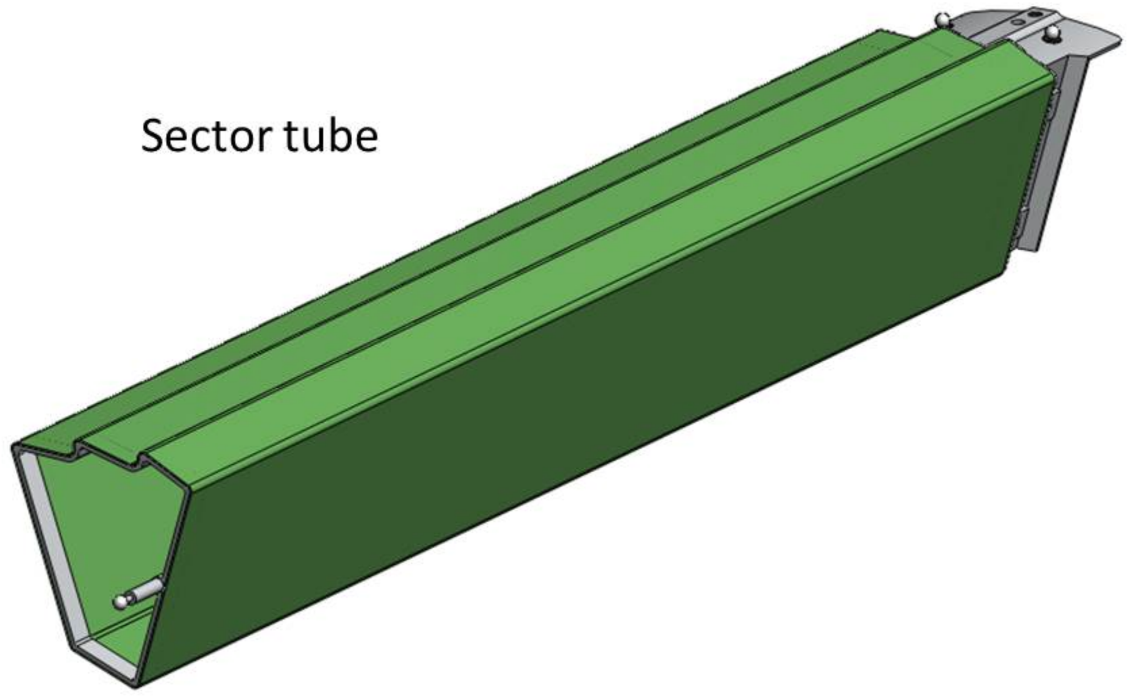


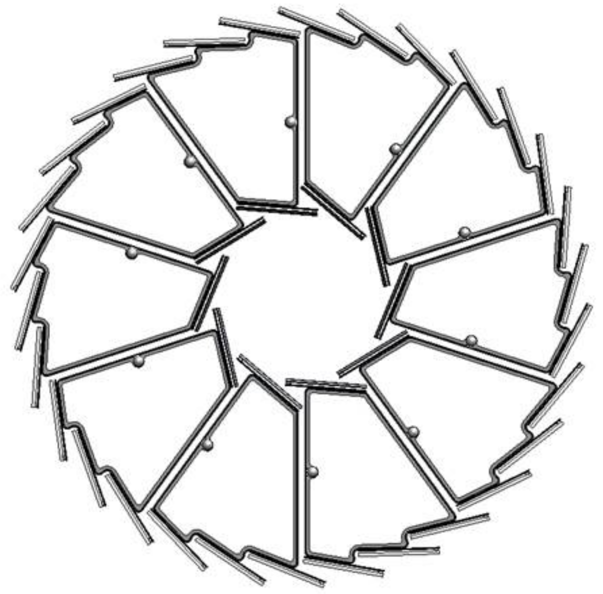
An amazing engineering masterpiece but NOT good enough for the next-gen lepton colliders since x/X_0 ~ 0.3%

✱ Something SMALLER & AIR COOLED: the STAR tracker @RHIC (OPERATIONAL since 2014)

- based on Monolithic Active Pixel sensors (MIMOSA-28), thinned to 50 μm
- pixel size: 20.7x20.7 μm^2
- TOTAL NUMBER OF PIXELS: 356 x 10^6 (400 sensors)
- **CHIP Power consumption: 170 mW/cm^2**
- **TOTAL POWER: 272W + 80W for the drivers**
- 2 layers @2.8 & 8 cm
- operated at room T + 10C

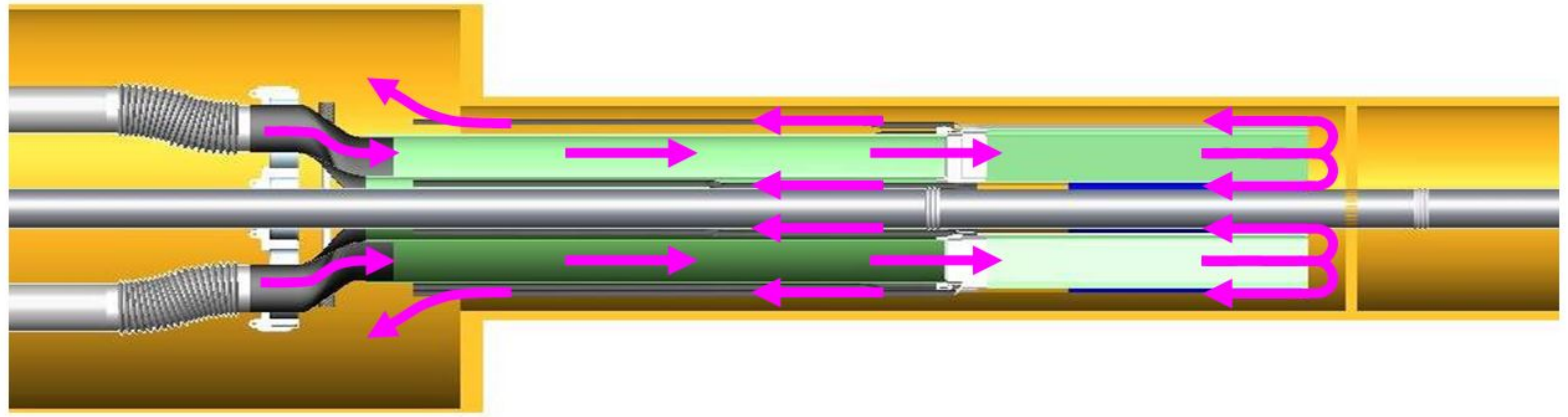






End view of detector

Carbon Fiber Sector, 120 μm thin

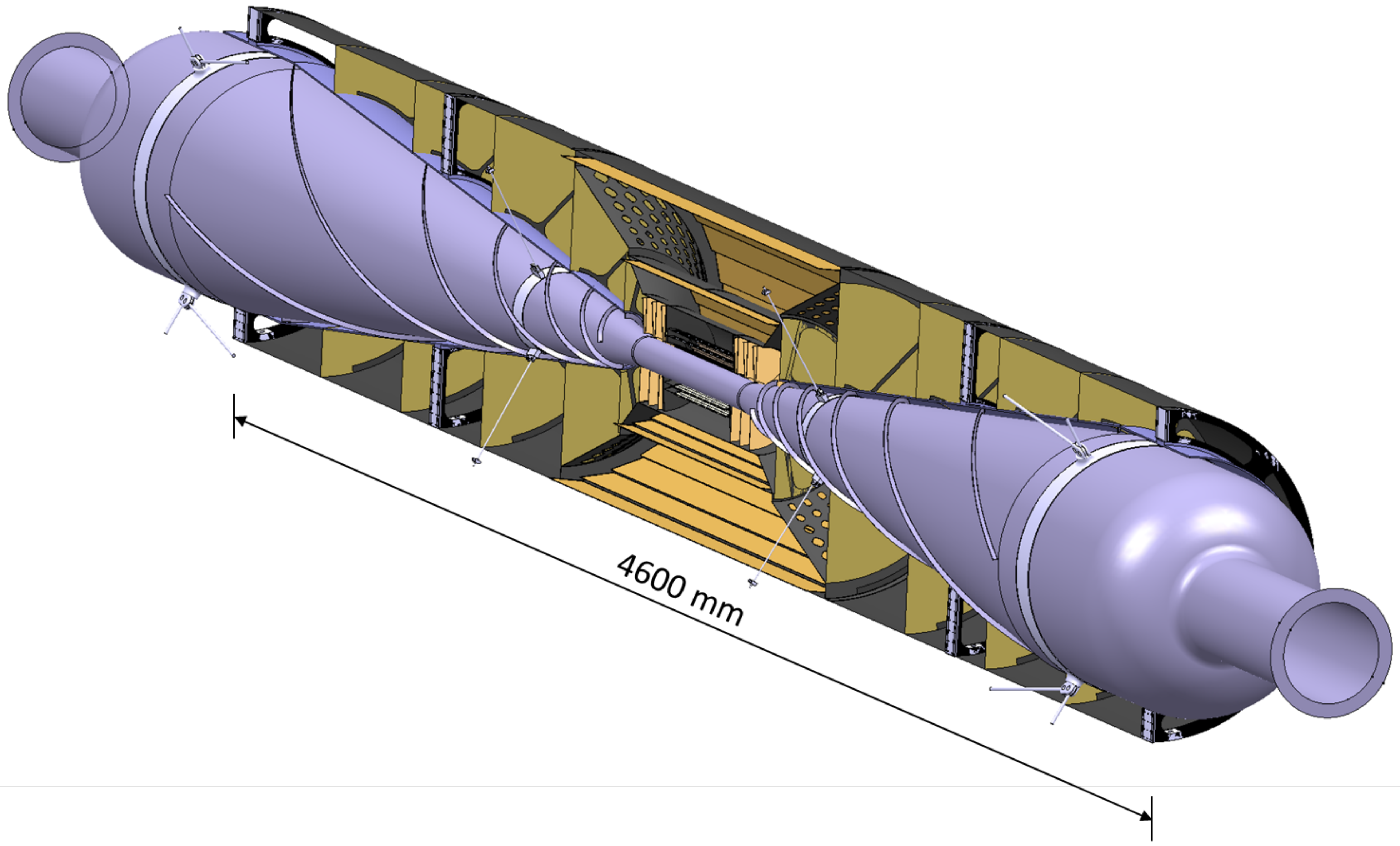


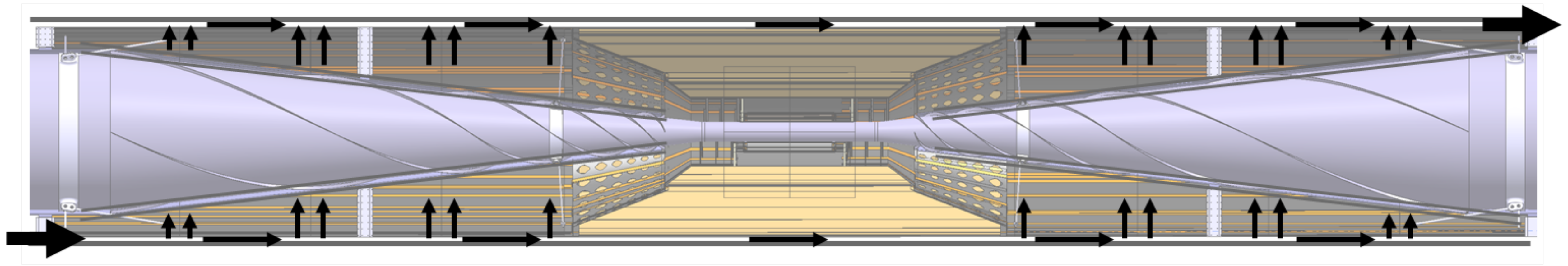
air flow at 10 m/s

STAR-HFT Heavy Flavour Tagger

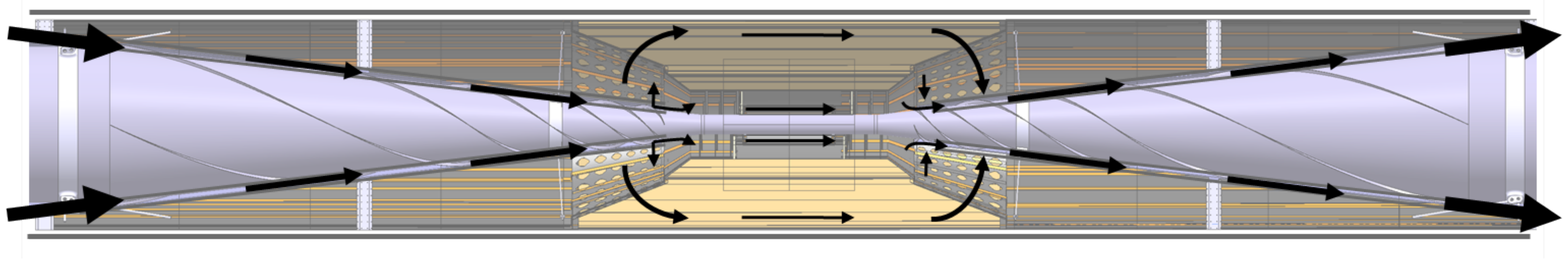
TOTAL MATERIAL BUDGET: 0.4% X0, for the 2 layers

✱ Something BIG & AIR COOLED: the CLIC-ILD tracker (will it ever be operational?)





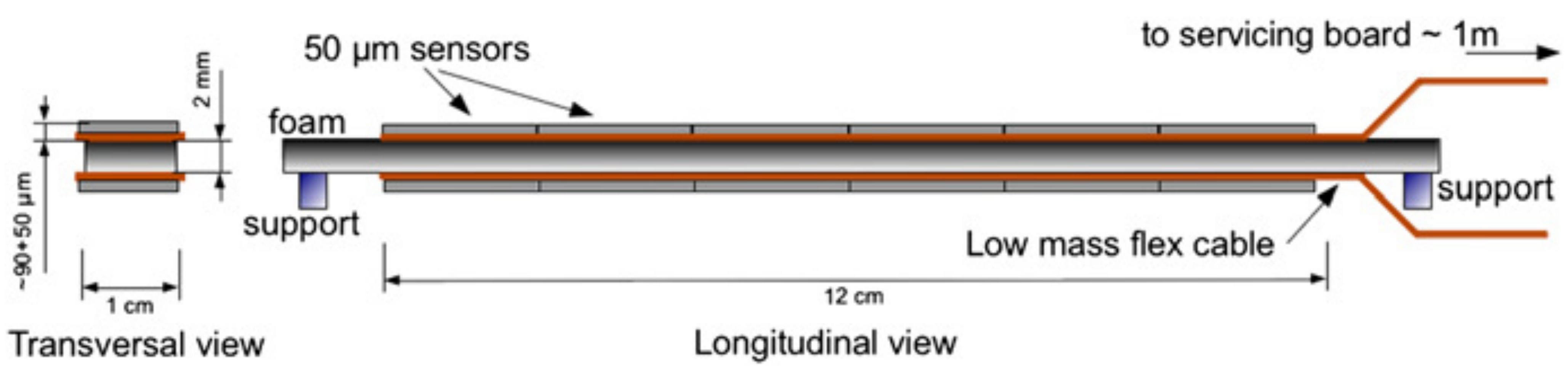
(a) Outer cooling stream



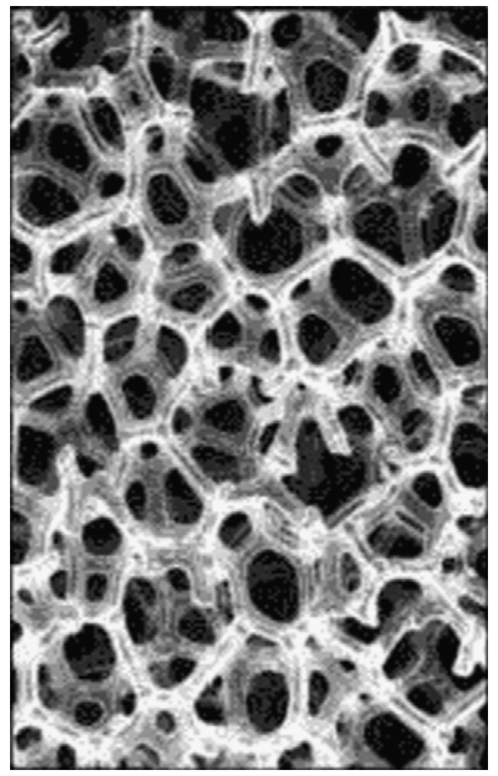
(b) Inner cooling stream

✱ Something "NEW" (1/3):

- PLUME (since 2009; initiated by the Strasbourg team) (AIR cooled oriented): a light weight support for the ILD double layer VTX design



SiC foam, about 2 mm thick

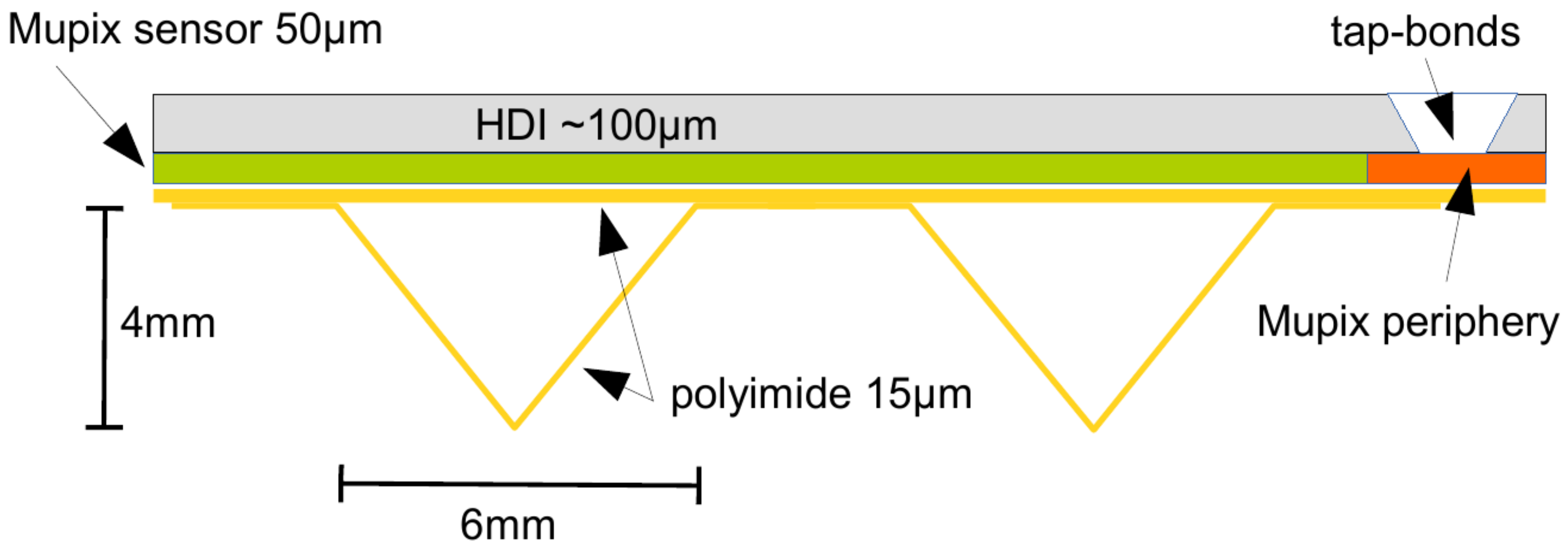


- Phase 1 (2009-2010):
  - fill factor 8% (1-void volume)/total volume
  - SiC foam: 0.18% X0
  - sensors: 0.11%
  - glue: 0.02%
  - flex cable: 0.29%
  - TOTAL: 0.6% X0
- Phase 2 (2011-2017)
  - investigating a lighter foam (4%), unfortunately brittle
  - characterising lower mass cables with Al or Cu traces

INTERESTING but slow progress and still not satisfactory

Something "NEW" (2/3):

AN ULTRA-LIGHT STRUCTURE FOR THE PIXEL TRACKER AT THE MU3E EXPERIMENT @PSI



	thickness [µm]	Layer 1-2 X/X_0	thickness [µm]	Layer 3-4 X/X_0
MuPix Si	45	$0.48 \cdot 10^{-3}$	45	$0.48 \cdot 10^{-3}$
MuPix Al	5	$0.06 \cdot 10^{-3}$	5	$0.06 \cdot 10^{-3}$
HDI polyimide & glue	45	$0.18 \cdot 10^{-3}$	45	$0.18 \cdot 10^{-3}$
HDI Al	28	$0.31 \cdot 10^{-3}$	28	$0.31 \cdot 10^{-3}$
polyimide support	25	$0.09 \cdot 10^{-3}$	≈ 30	$0.10 \cdot 10^{-3}$
adhesives	10	$0.03 \cdot 10^{-3}$	10	$0.03 \cdot 10^{-3}$
total	158	$1.15 \cdot 10^{-3}$	163	$1.16 \cdot 10^{-3}$

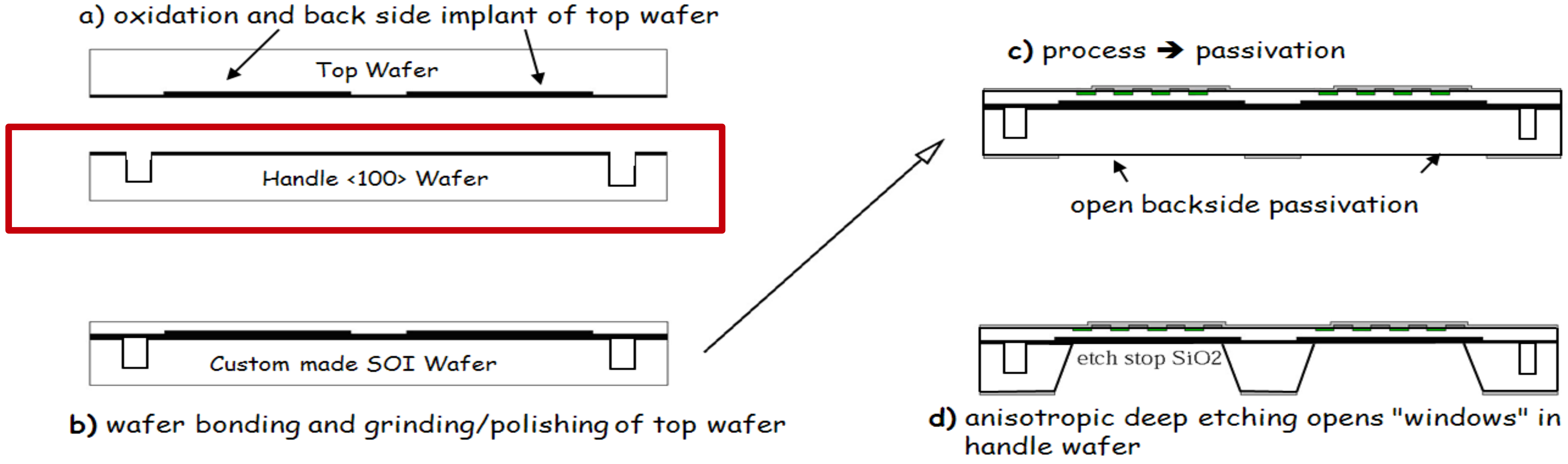
Cross section of the High Density Interconnection layer:

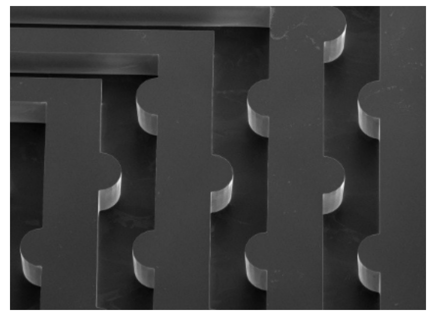
Material	Thickness [µm]	X/X0
⇒ upper Al layer	14	$1.57 \cdot 10^{-4}$
isolator (PI)	35	$1.22 \cdot 10^{-4}$
glue	10	$0.25 \cdot 10^{-4}$
⇒ lower Al layer	14	$1.57 \cdot 10^{-4}$
lower PI shield	10	$0.35 \cdot 10^{-4}$
total	83	**$< 5 \cdot 10^{-4}$**

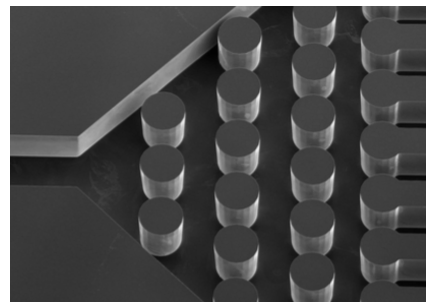
A 36cm long mock-up, equipped with 50 µm glass layers mimicking the pixels

✱ Something "NEW" (3/3):

▷ ALL-SILICON MODULES WITH INTEGRATED COOLING CHANNELS (initiated by MPG-HLL Munich + Bonn + Valencia/P. Petagna @CERN)

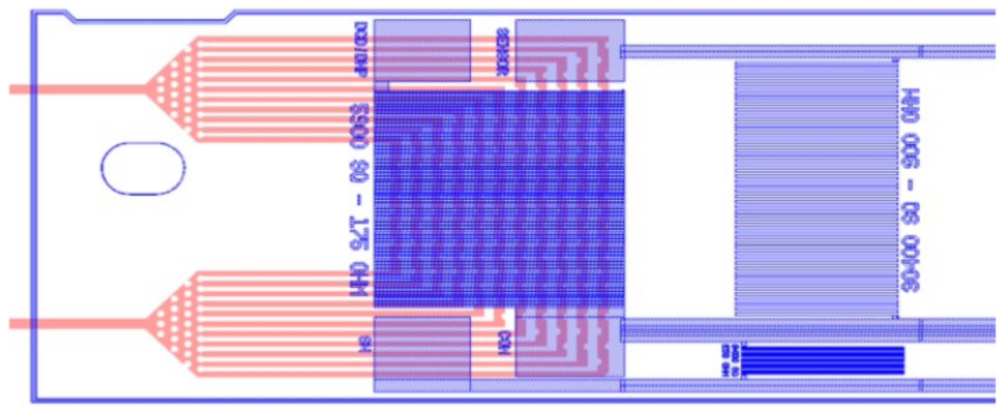


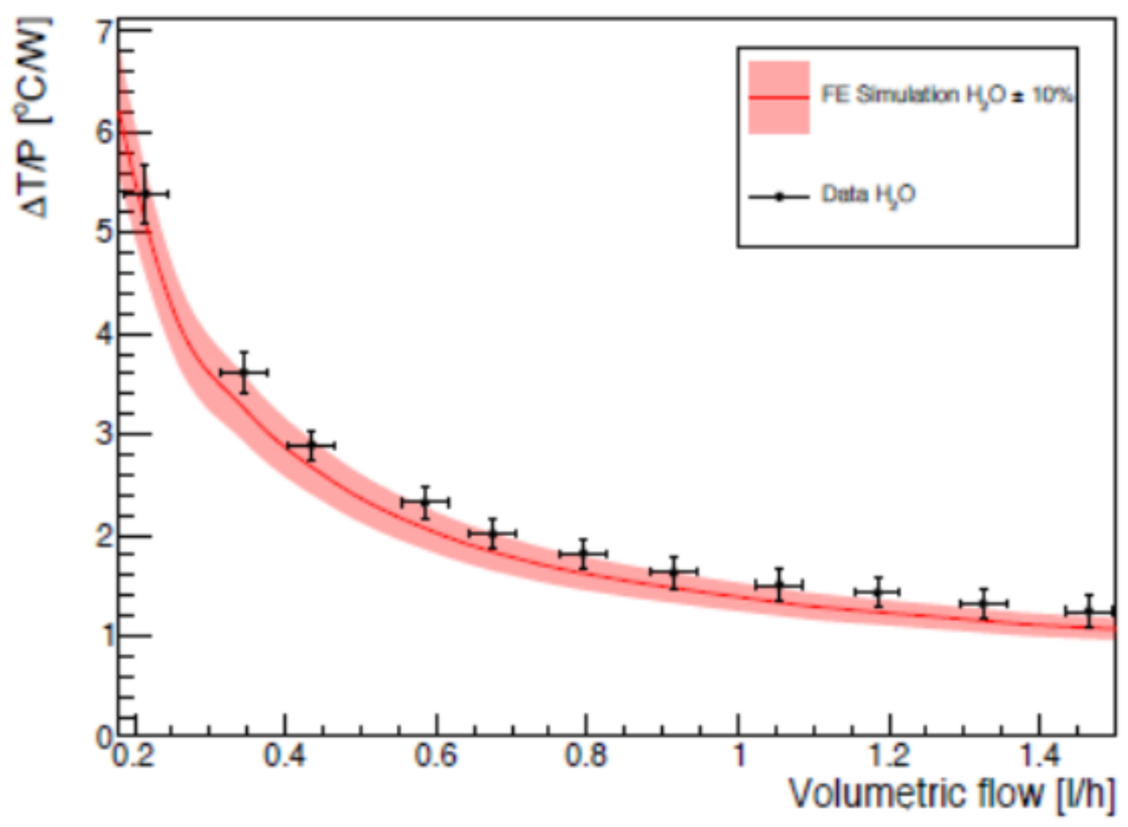


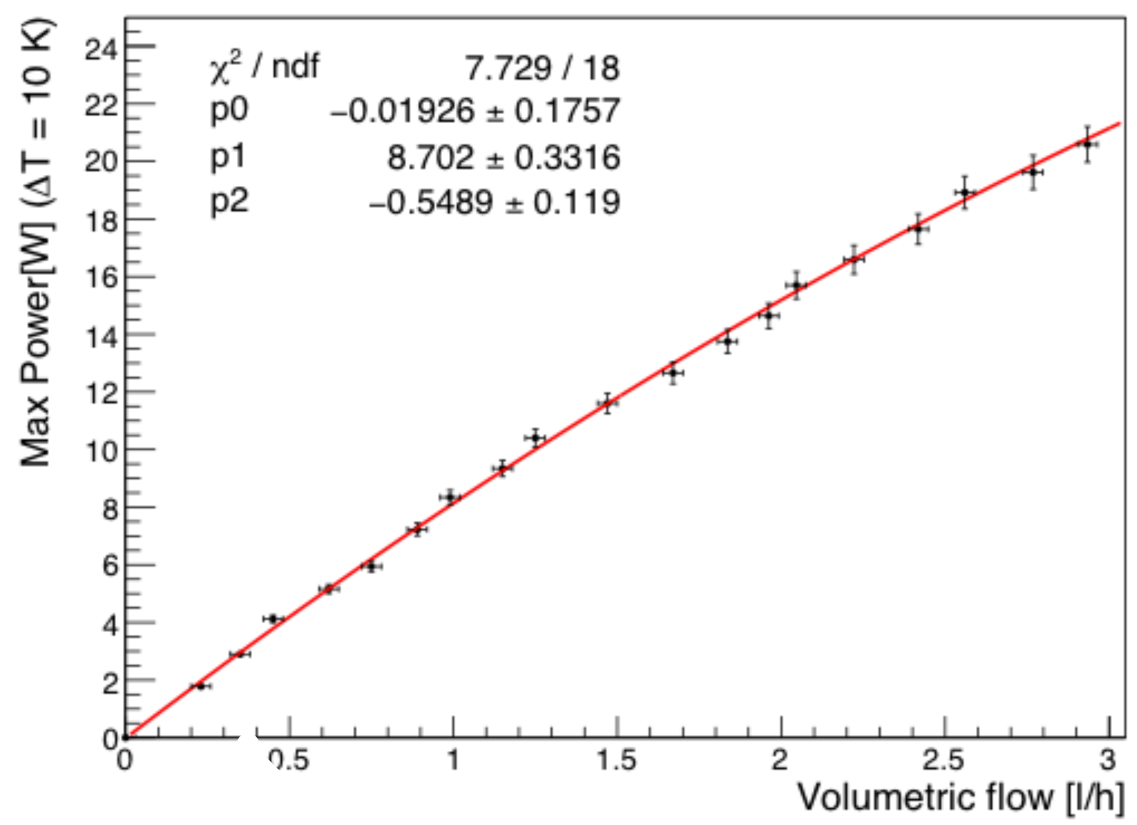


process a pattern of cooling channels in the handle wafer of the assembly

Results by a test module:



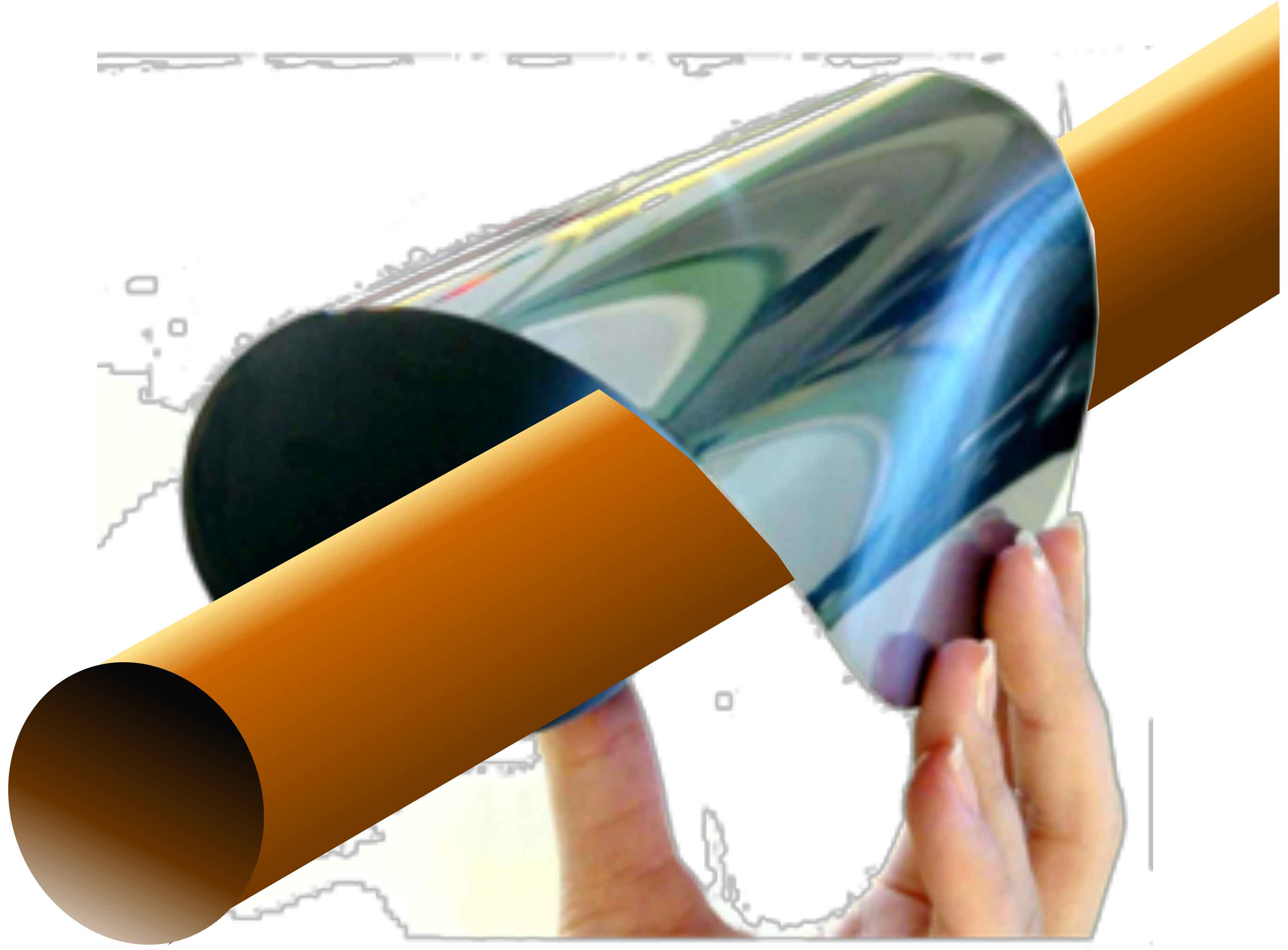




✱ A popular view (which I fully subscribe):

If air cooling works:
(namely if I have a power density **~ 20 mW/cm²**)

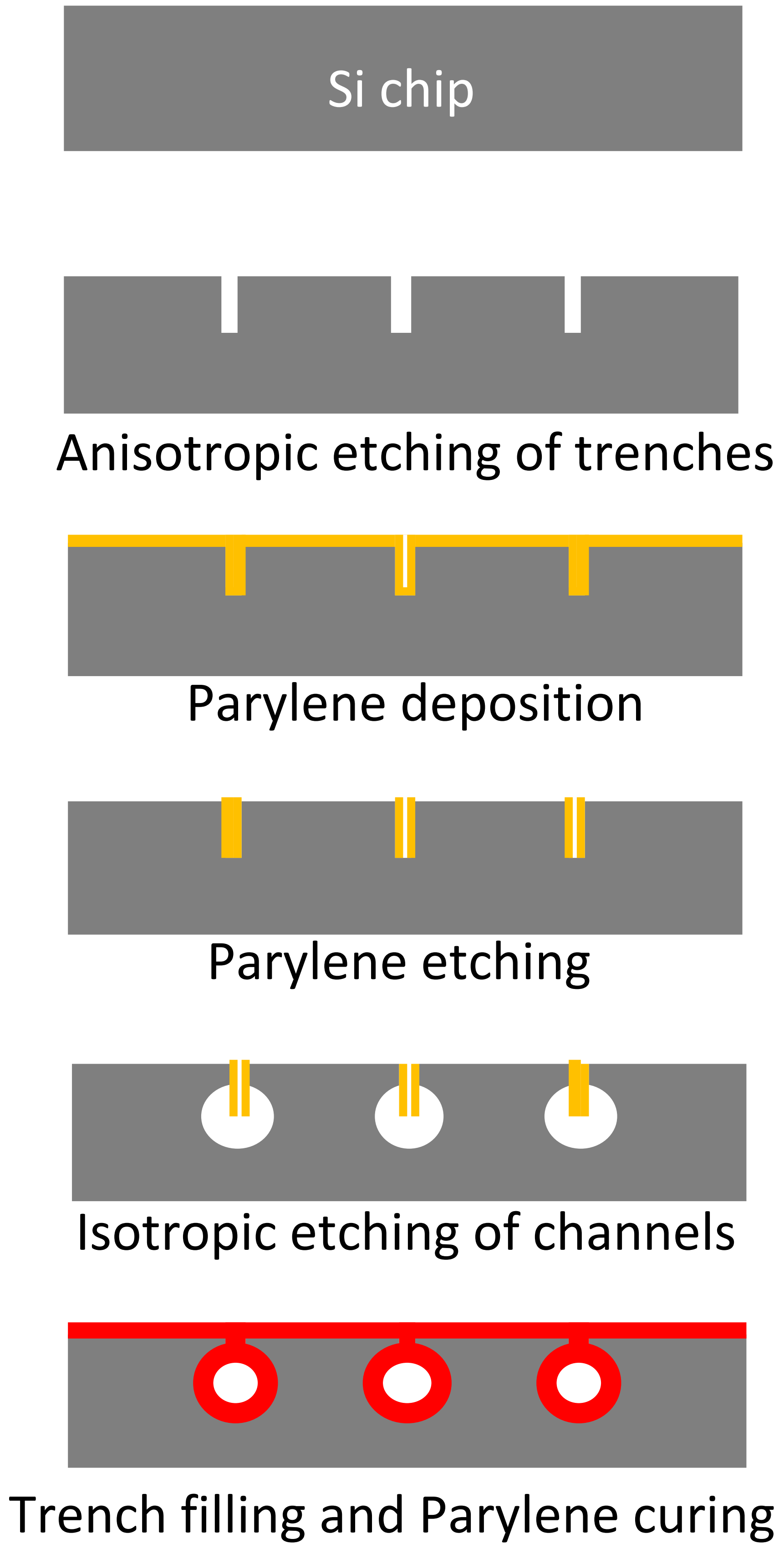
from C. Gargiulo's CERN seminar



- ✓ ***Eliminate liquid cooling***
  possible for power <20mW/cm2
- ✓ ***Eliminate electrical substrate***
  possible if the sensor covers the full stave length: ***Stitching***
- ✓ ***Minimize mechanical support***
  exploit flexible nature of the silicon (<50µm): ***Bending***

Otherwise:

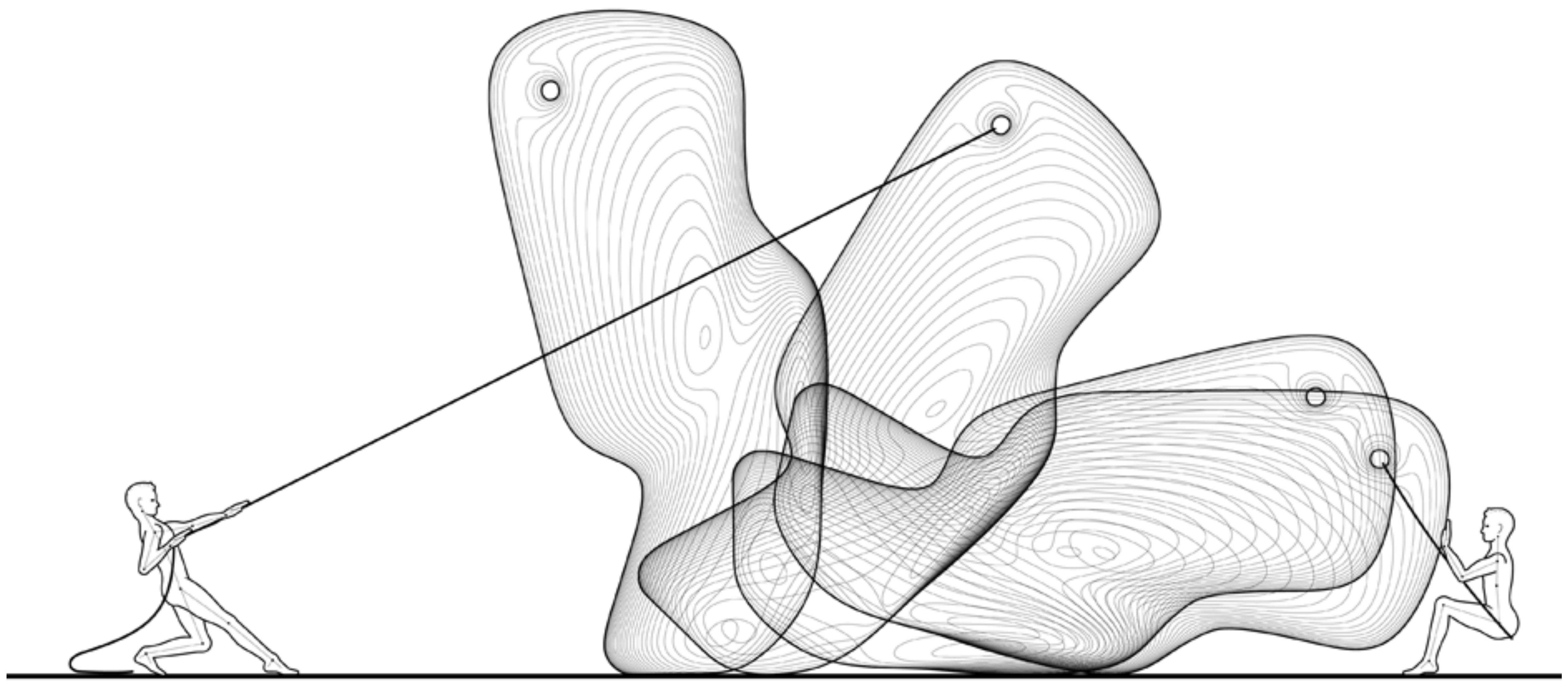
Integrate the microchannels in the back of the Detector



3. SENSORS, ENFIN!

where CONCEPT, TECHNOLOGY & ARCHITECTURE do matter

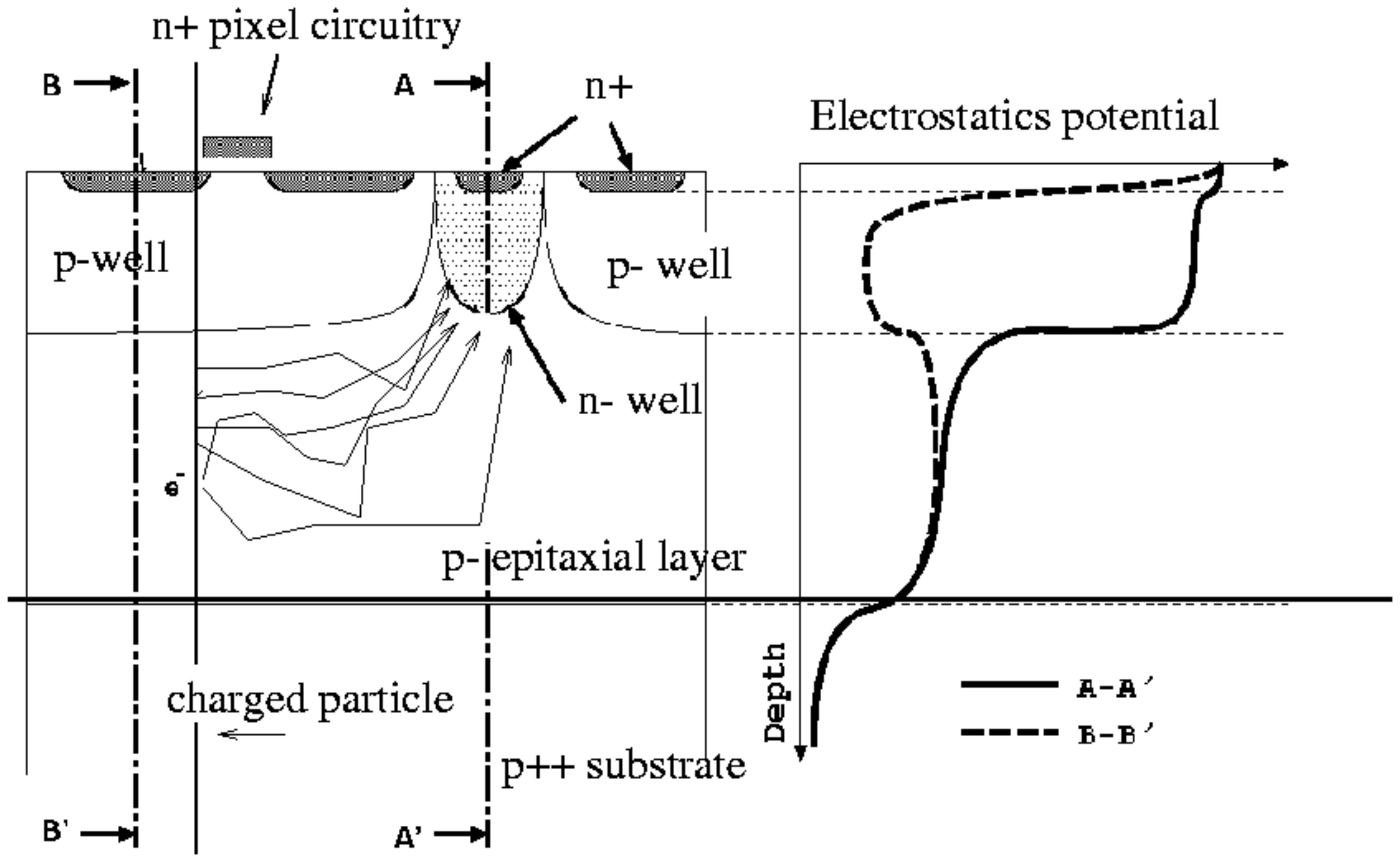
* Talking about **CONCEPTS**, I would certainly go **MONOLITHIC**, or at least **SEMI-MONOLITHIC:**



MIT students create 2,000-pound "megalith" that can be moved with a fingertip

https://www.dezeen.com/2015/11/13/massachusetts-institute-of-technology-mit-students-mckneely-megalith-sculptural-object-balance/

Monolithic Active Pixel Sensors (MAPS), namely CMOS sensors for particle detection



❖ Main drive from digital cameras

❖ Pioneered @ LEPSI Strasbourg in the late 90's:

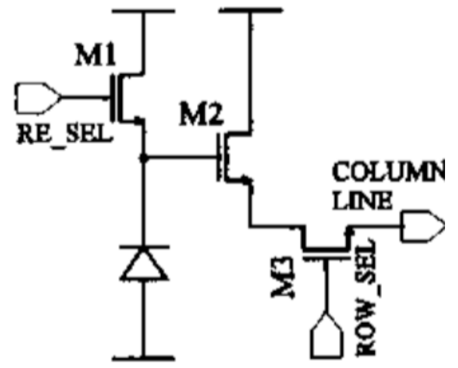
- G. Deptuch at al, IEEE-TNS 49 (2002) 601
- R. Turchetta et al, NIM A458 (2001) 677

NON STANDARD SENSORS [early days specs!]:

- based on the charge carrier generated in the epitaxial layer [2-14 μm thick, depending on the technology => SMALL signal (~80 e-h pairs/ μm)]
- diffusion detector vs [standard] drift sensors (the sensitive volume is NOT depleted => charge cluster spread over ~ 100 μm [10 μm] AND collection over ~ 150 ns [10 ns])

NEVERTHELESS OFFERING SEVERAL ADVANTAGES:

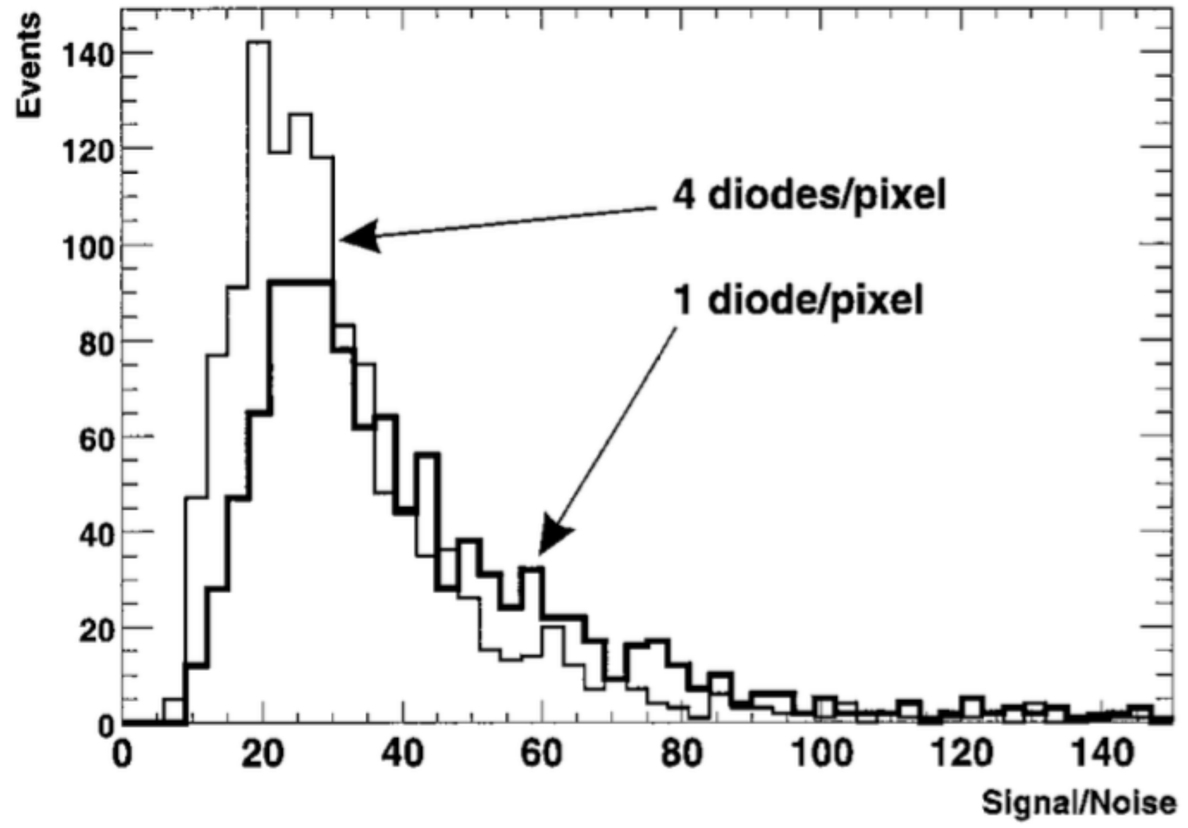
- very simple baseline architecture (3Transistors: reset, source follower, address key)



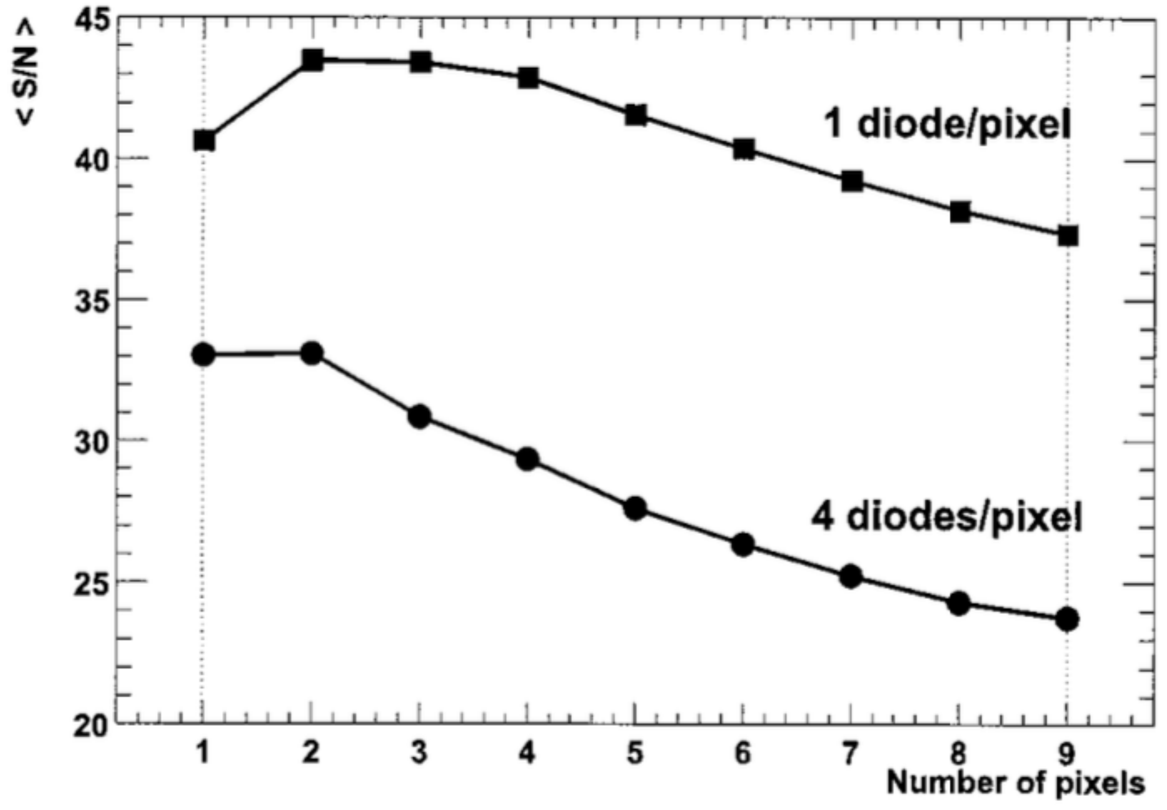
- standard, well established industrial fabrication process, granting a cost-effective access to state-of-the-art technologies, including **back thinning**

Early 2019 estimate of the cost for the LFoundry process: about 160 EUR for a sensor with reticle size area, e.g. 25x30mm²

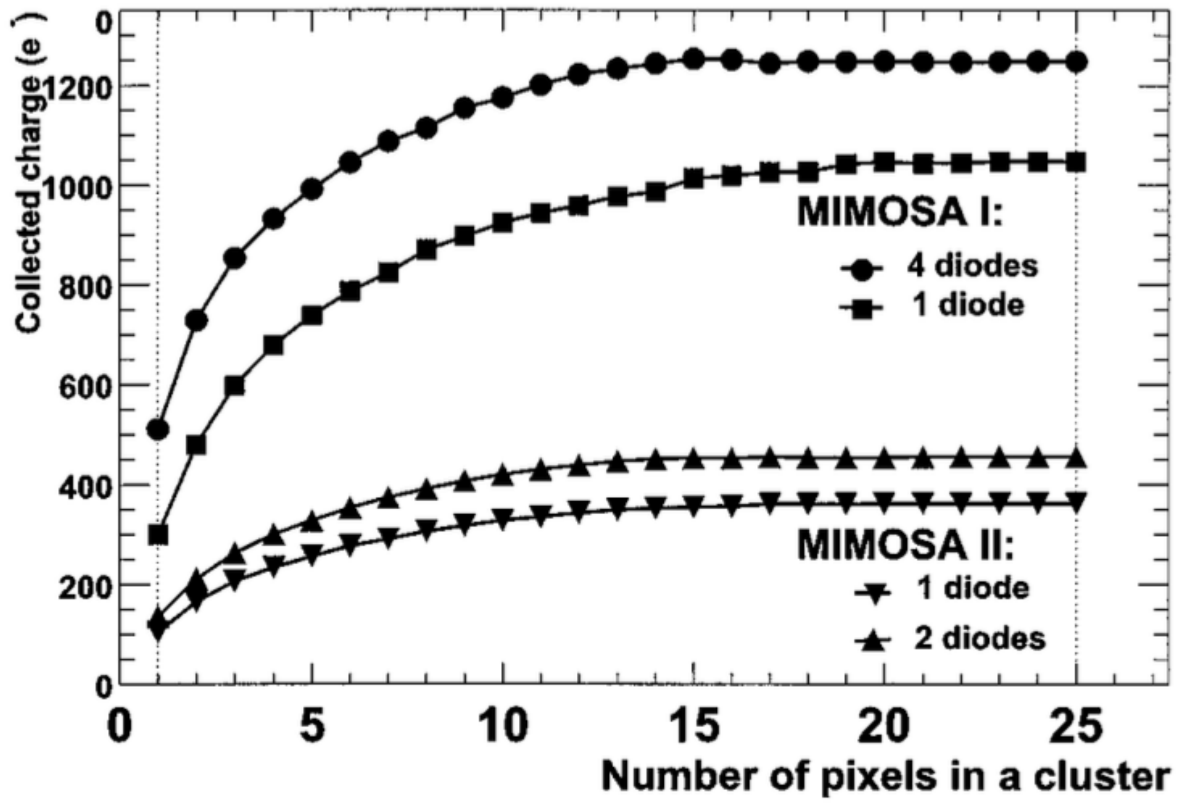
A tribute to the Strasbourg team; early results from the MIMOSA (Minimum Ionising particle MOS Active pixel sensors) 1 & 2 (back to 2002):



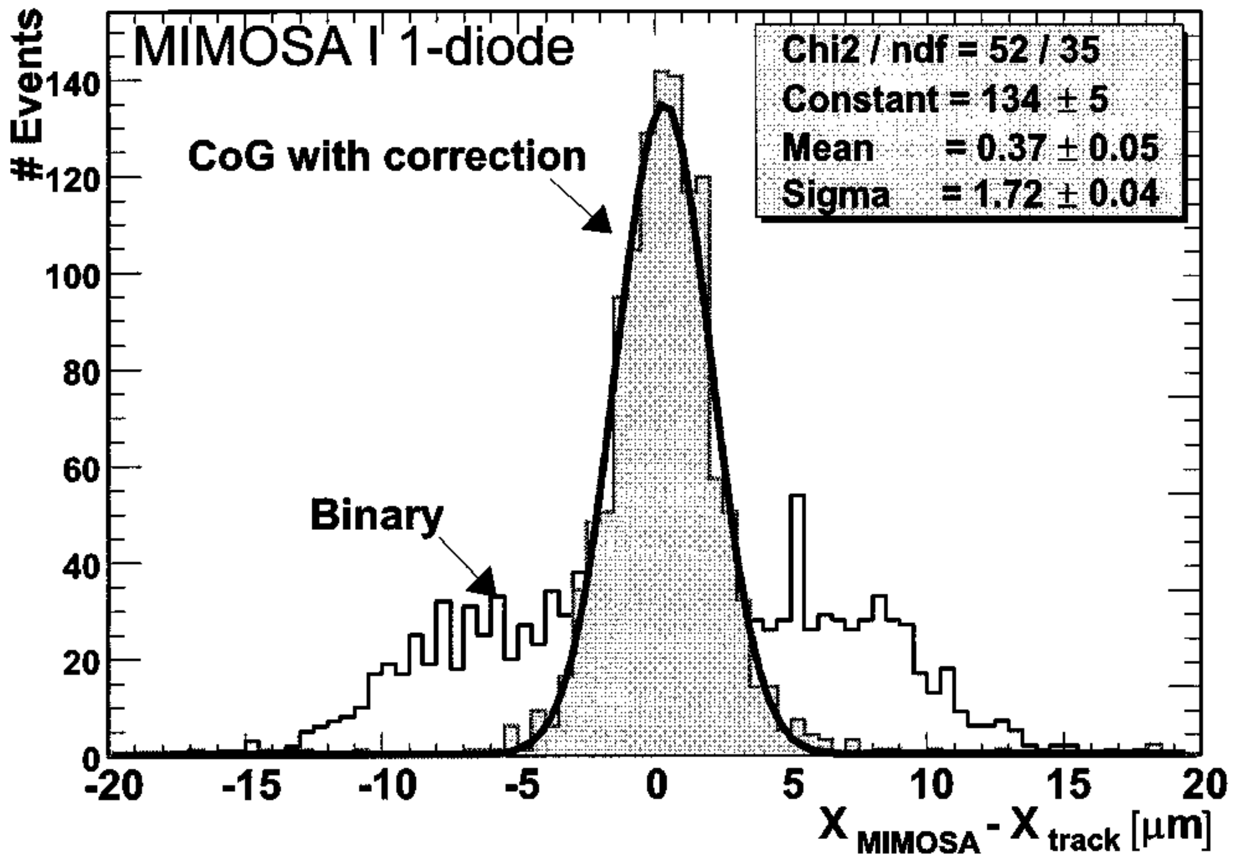
S/N for the seed pixel



S/N vs cluster size



Collected charge vs no. pixels



Resolution

AMS 0.6 μm technology - 14 μm epitaxial layer - 20 μm pixel pitch

SEMI-Monolithic Pixels: the DEPFET (DEPleted Field Effect Transistors) [see talk by Laci Andricek]

Sideward depletion when

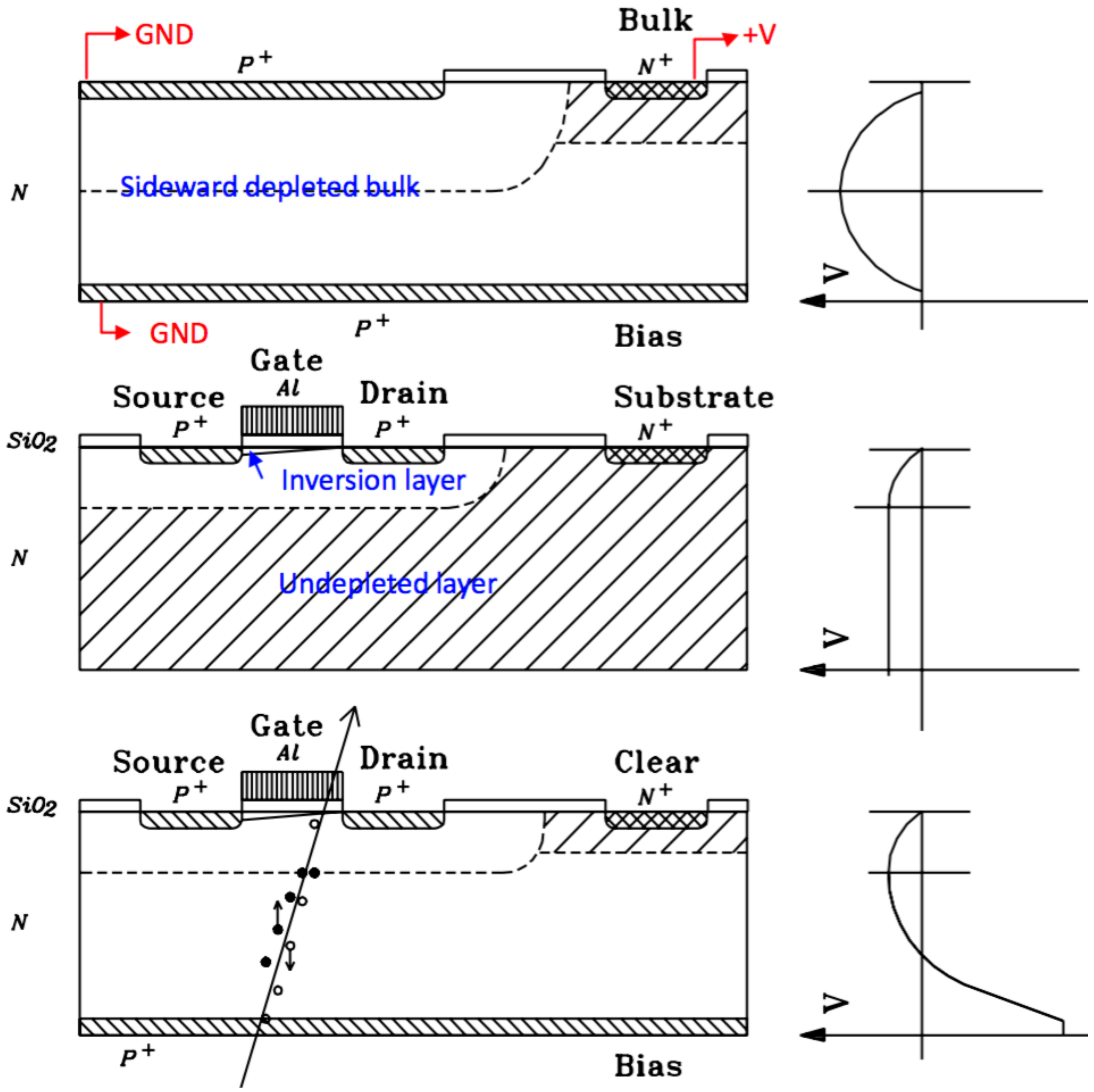
- diodes are located on both sides of a wafer
- substrate contact, located on the side, is polarized in the reverse bias direction with respect to the large-area diode junction
- A potential minimum for majority carriers (electrons in n-type silicon) forms between the two diode junctions.

MOS transistor

- A standard MOS enhancement-type transistor built on top of the bulk
- Conductivity of the channel steered not only by the gate voltage but also by the bulk potential.

DEPFET detector

- Bias applied on back side – minimum valley moves toward FET channel
- Holes moves toward back side
- Electrons toward the potential valley
- Mirrored charge in the FET gate open the channel and current flows.
- Positive signal applied to Clear electrode moves away electrons from valley and close the FET channel



internal gain 500 pA/e

© L.Rossi et al. [ref. b]

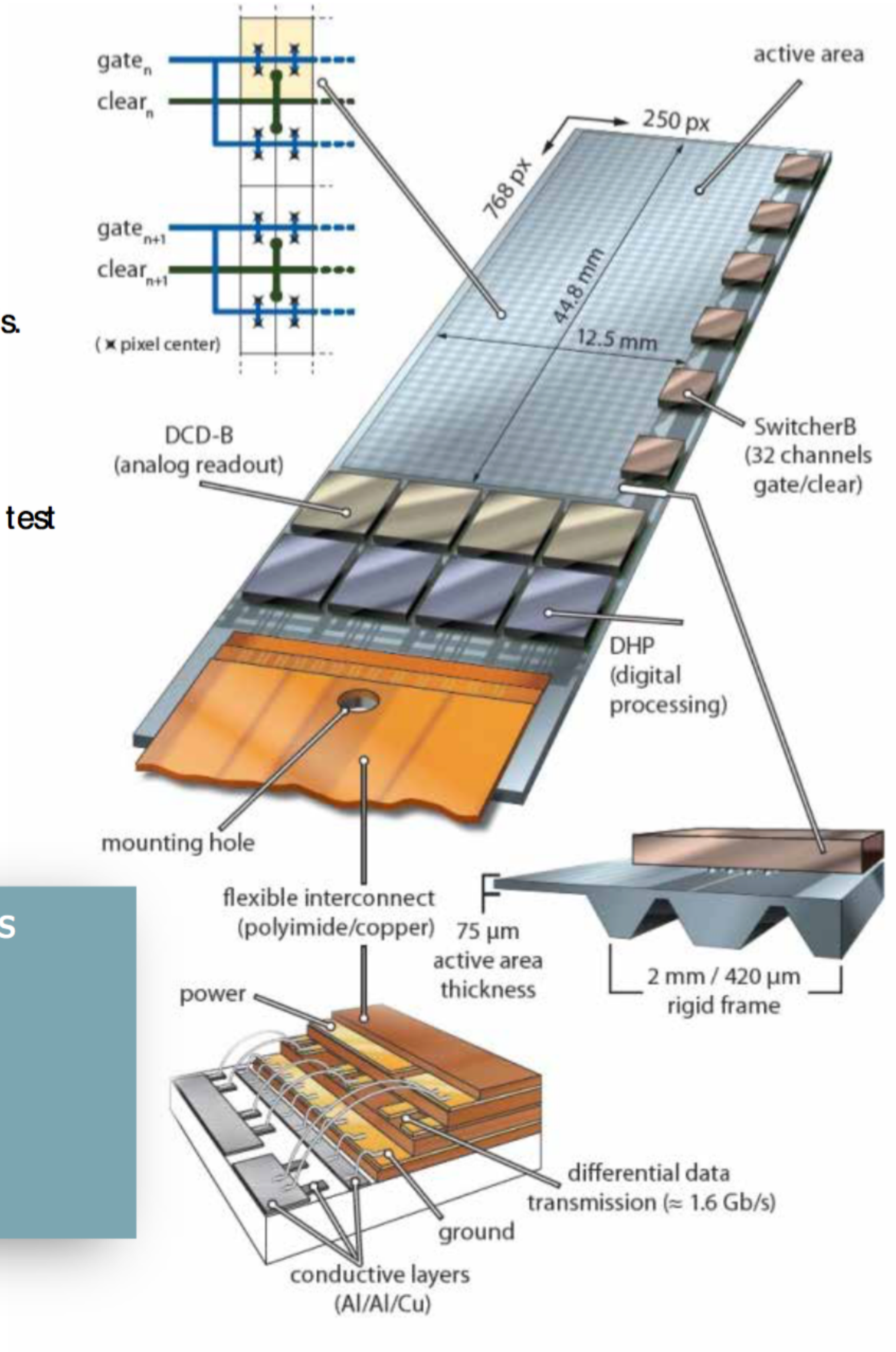
a. L.Rossi, T.Rohe, P.Fischer and N.Wermes, **Pixel Detectors - From Fundamentals to Applications**. Springer, 2006.

DEPFET: an all-Silicon module (but exactly monolithic)

DCDB (Drain Current Digitizer)
Analog front-end

Amplification and digitization of DEPFET signals.

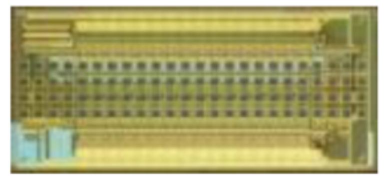
256 input channels
8-bit ADC per channel
92 ns sampling time
new version **w/ 50ns** sampling time under test
UMC180 nm
Rad hard design



Key to low mass vertex detectors

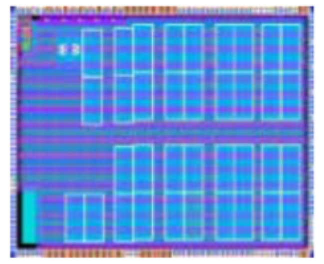
highest integration!
Thin sensor area
EOS for r/o ASICs
(perforated) silicon frame
w/ steering ASICs

SwitcherB - Row Control



AMS/IBM HVCMOS 180 nm
Size 3.6 · 1.5 mm^2
Gate and Clear signal
32x2 channels
Fast HV ramp for Clear
Rad. Hard proved (36 Mrad)

DHP (Data Handling Processor)
First data compression



TSMC65 nm
Size 4.0 · 3.2 mm^2
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing and trigger control
Rad. Hard proved (100 Mrad)

and the experience with the BELLEII Vertex detector is certainly beneficial:

	ILD LOI 5-layer layout	Belle II	
Radii	15, 26, 38, 49, 60	14, 22	mm
Sensitive length	123 (L1), 250 (L2-L5)	90 (L1), 122 (L2)	mm
Sensitive width	13 (L1), 22 (L2-L5)	12.5 (L1-L2)	mm
Number of ladders	8, 8, 12, 16, 20	8, 12	
Pixel size	20x20 (L1-L5)	55x50 & 60X50 (L1), 70x50 & 85x50 (L2)	µm^2
r/o time per row	50 (L1), 250 (L2-L5)	100	ns
Number of pixels	800	8	Mpix

	Belle II pixel detector	ILD vertex detector
Occupancy [hits/μm^2/s]	0.40	0.13
TID per year [Mrad]	2.0	< 0.1
NIEL per cm^2 and year [1 MeV n$_{eq}$]	2.0×10^{12}	1.0×10^{11}
Frame readout time [μs]	20	25–100
Material budget per layer [X$_0$]	0.21 %	0.12%
Pixel pitch [μm^2]	50×75	20×20
Resolution [μm]	15	5

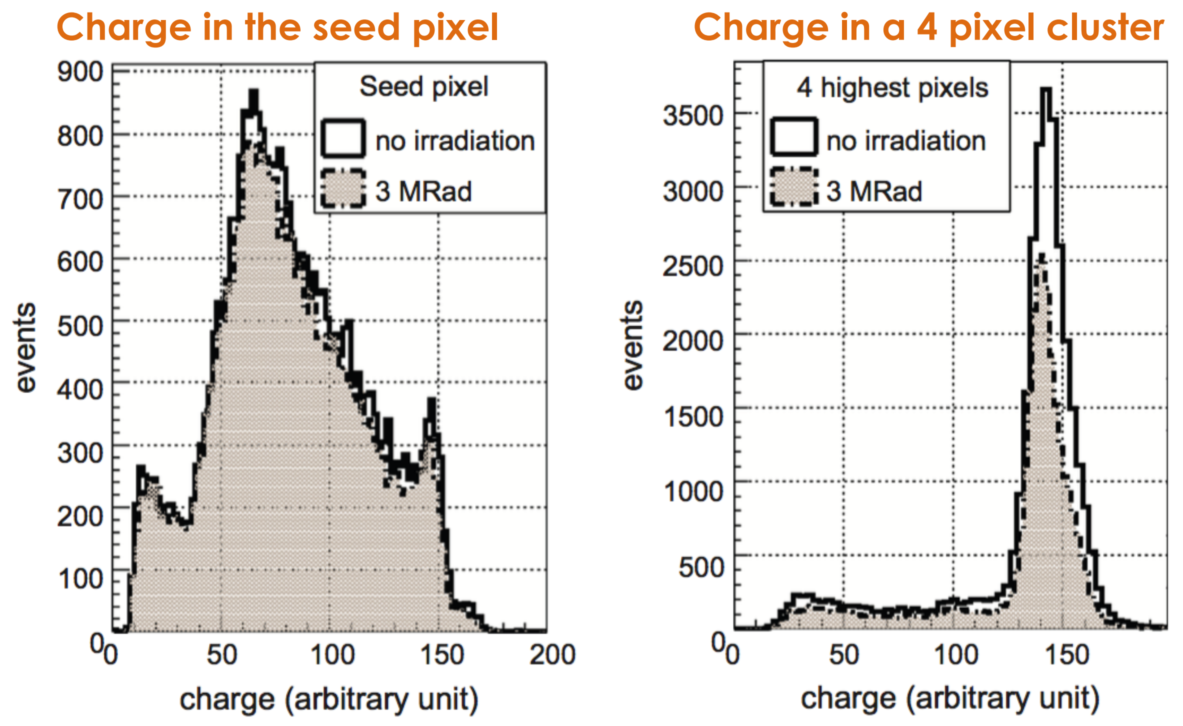
Talking about **TECHNOLOGY**, we could be discussing for ages:

- **An incomplete inventory of technologies/processes used so far:**
  - epi- less technologies (AMS 350 nm)
  - low resistivity epitaxial layer, bulk (large catalogue)
  - low resistivity epitaxial layer, OPTO tech (AMS 350 nm)
  - low resistivity epitaxial layer, 3 wells (e.g. STm 130 nm)
  - low resistivity epitaxial layer, 4 wells (e.g. INMAPS)
  - **High Resistivity epitaxial layer, 4 wells (e.g. Tower Jazz 180 nm)**
  - **SOI on High resistivity Substrate (LAPIS, formerly OKI)**
  - Vertical integration (e.g. Tezzaron)
  - **Full CMOS on high resistivity substrates (LFoundry)**

low resistivity: ≈ 10 Ω cm, collection by diffusion
high resistivity > 1 k Ω cm, collection by drift

- **What I know, is that I would rather choose a high resistivity substrate:**

1. smaller charge spread & cluster



G. Baudot at al, NIM A732 (2013) 480

TJ 0.18 μm technology - 18 μm epitaxial layer - 20 μm pixel pitch, illuminated by an 55fe source (5.9 keV X ray, generating 1640 eh pairs

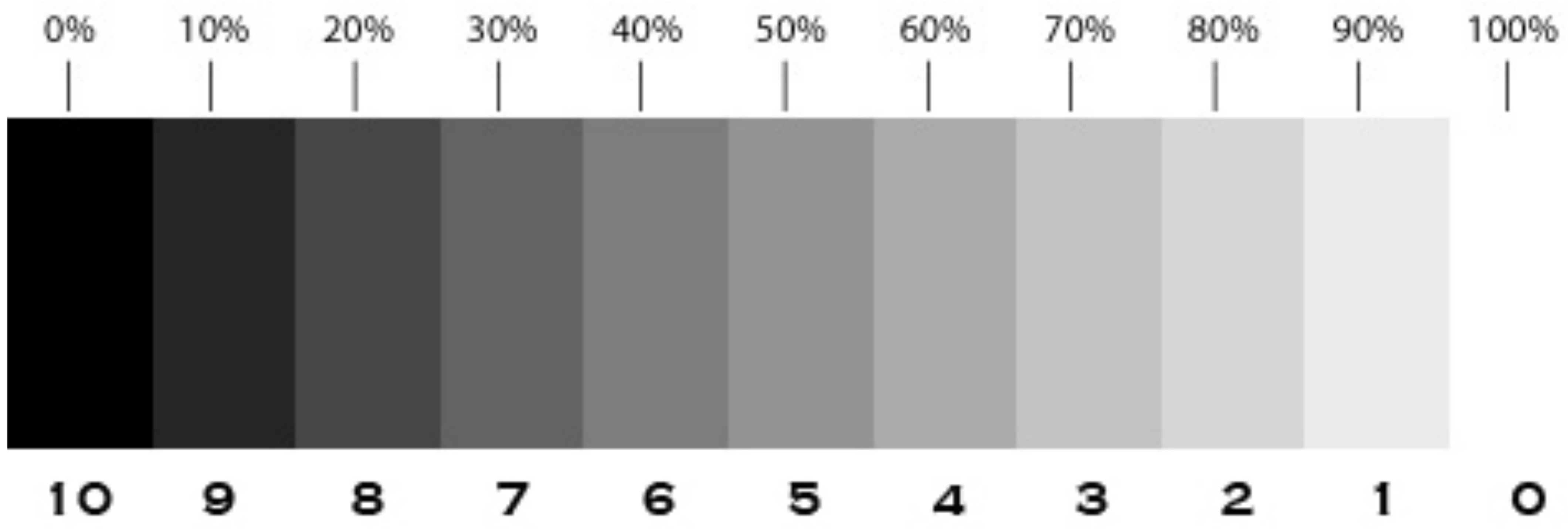
2. shorter collection time ⇢ reduced trapping probability ⇢ increased radiation tolerance (possibly from 10^{12} n_{eq}/cm^2 to 10^{15} n_{eq}/cm^2 [W. Snoeys, NIM A731 (2013) 125]

3. possibility to design pixels with unusual aspect ratio ⇢ SHORT STRIPS (e.g. Z. Liang et al., NIM A (2016) http://dx.doi.org/10.1016/j. nima.2016.05.007)

AND THERE IS A GROWING ACTIVITY HERE!

Moving on to **ARCHITECTURE**, I would consider at least 2 features:

1. Pixels can be ANALOG

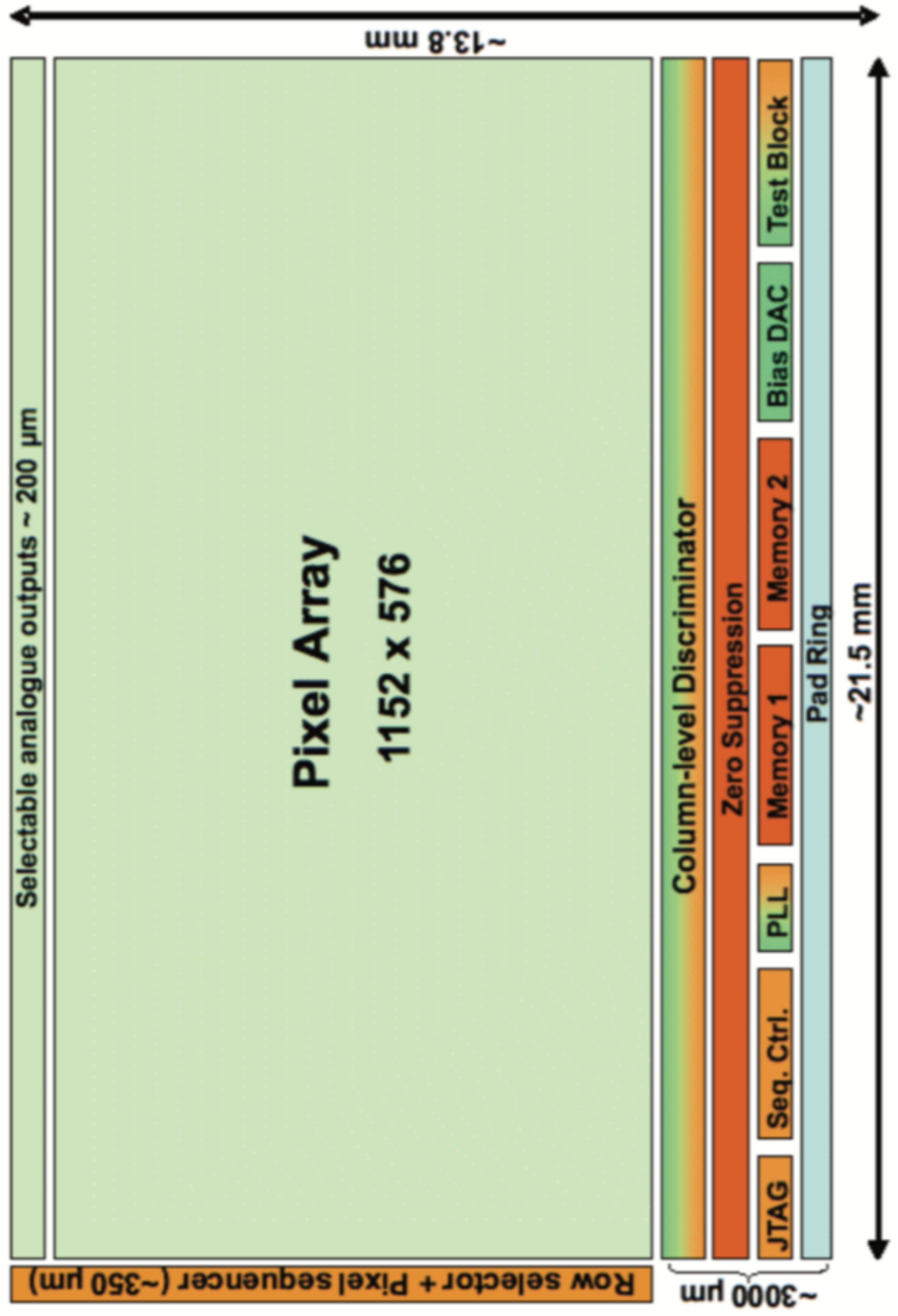


or BINARY:

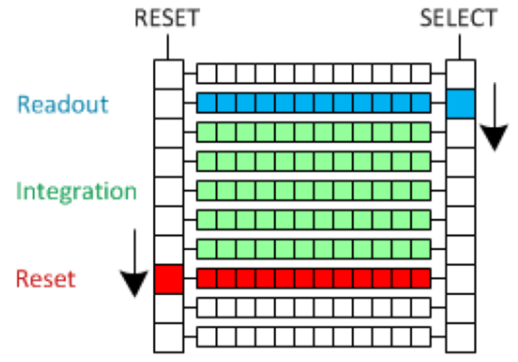
Moving on to **ARCHITECTURE**, I would consider at least 2 features:

Since the pitch/√12 rule has been violated in MAPS....

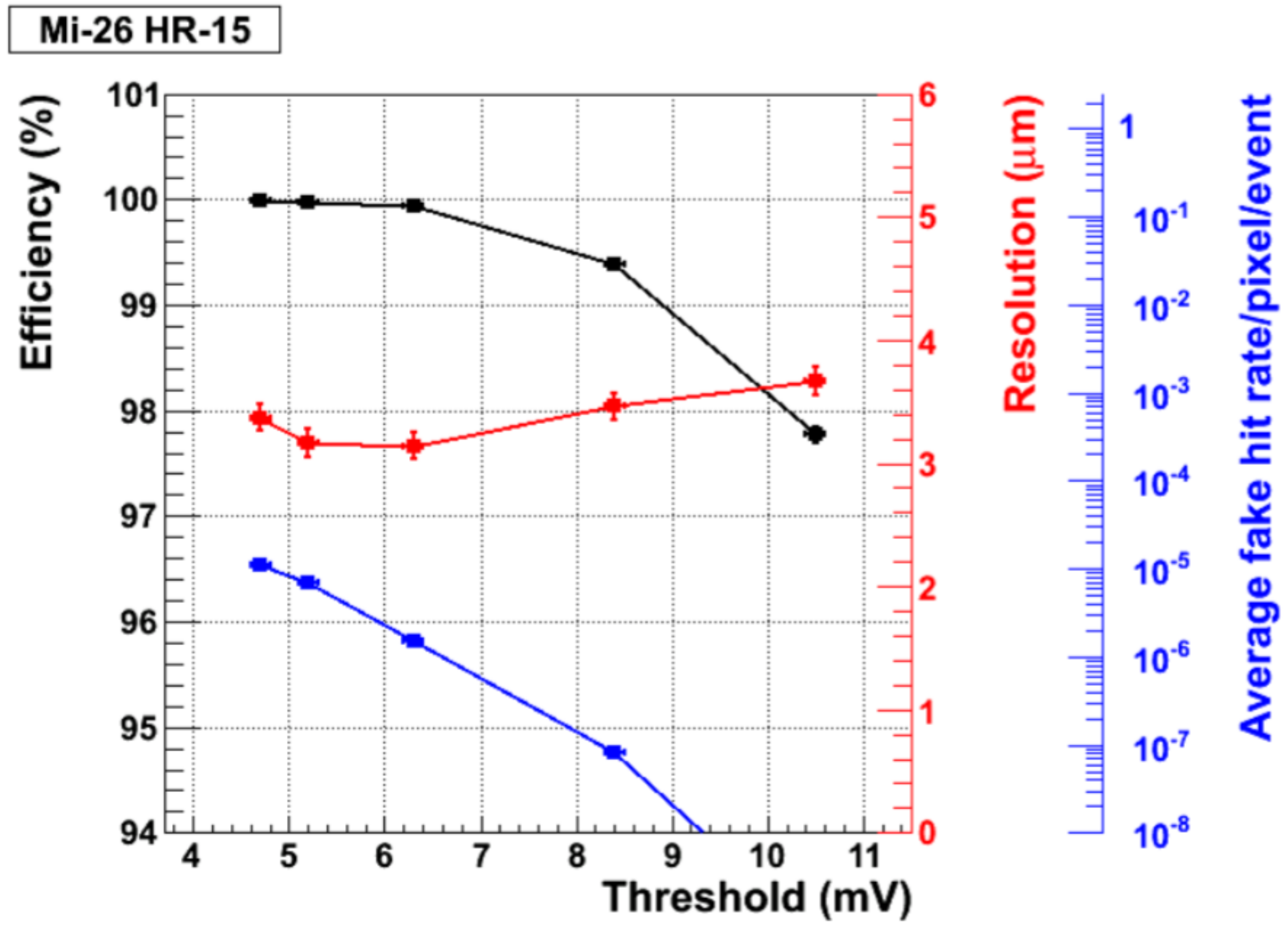
The MIMOSA26, an architecture for the high spatial resolution innermost layer at the ILC [J. Baudot et al., IEEE-NSS 2009 conf. record]:



- reticle size detector, 0.35 µm OPTO
- on pixel correlated double sampling & ampli
- rolling shutter & parallel column readout



- binary output - 18.4 µm pitch
- sensor readout in 112 µs (80 MHz clock) (200 ns/pixel)
- fake hit rate 10^{-4} / pixel
- efficiency 99.5 +/- 0.1 %
- power consumption: 520 µW/column => 700 W for the full VD (150 mW/cm^2)
- thinned down to 50 µm (et la PLUME!)



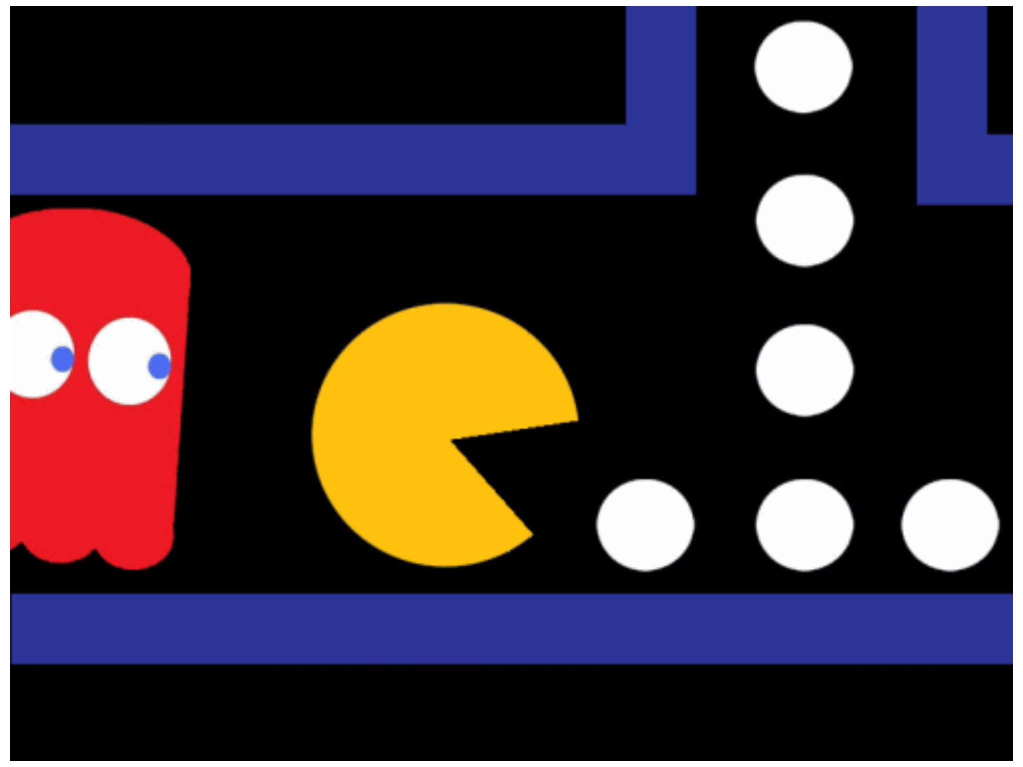
M. Winter et al., arXiv: 1203.3750v1 (2012)

- **binary resolution = 18.4/√12 = 5.3 µm**
- **measured resolution; 3.5 µm**

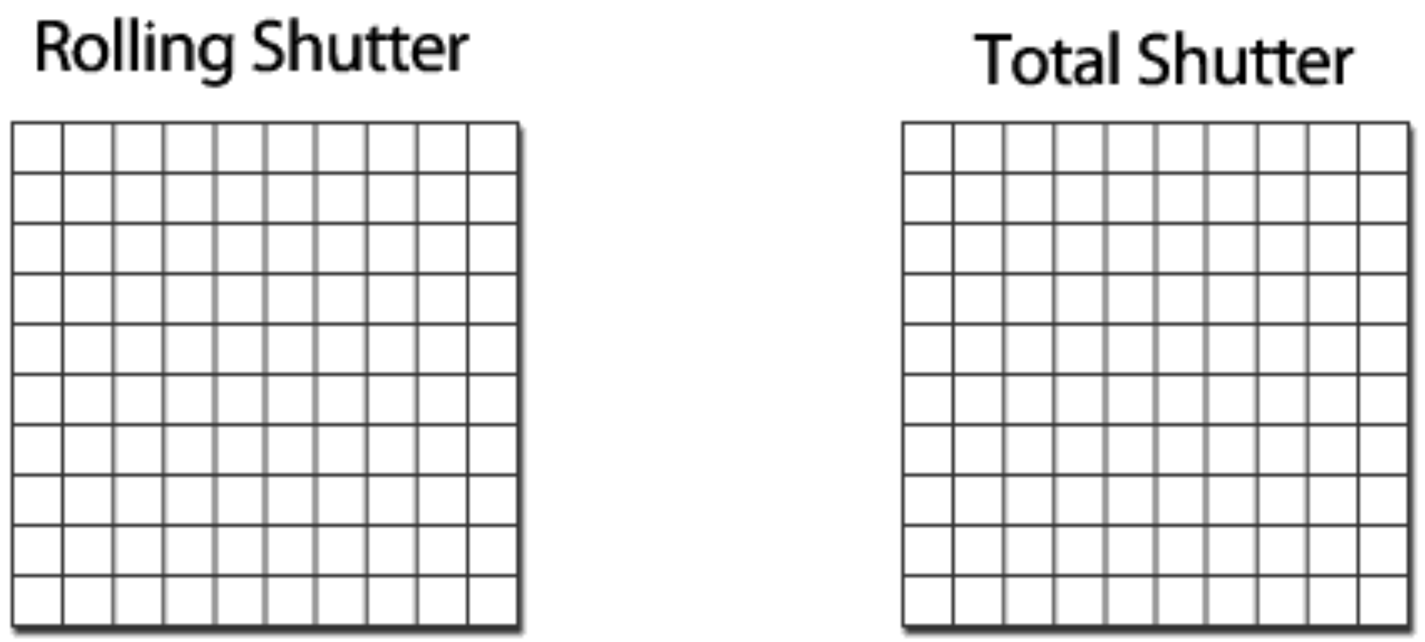
... I would certainly go for BINARY pixels

✱ Moving on to **ARCHITECTURE**, I would consider at least 2 features:

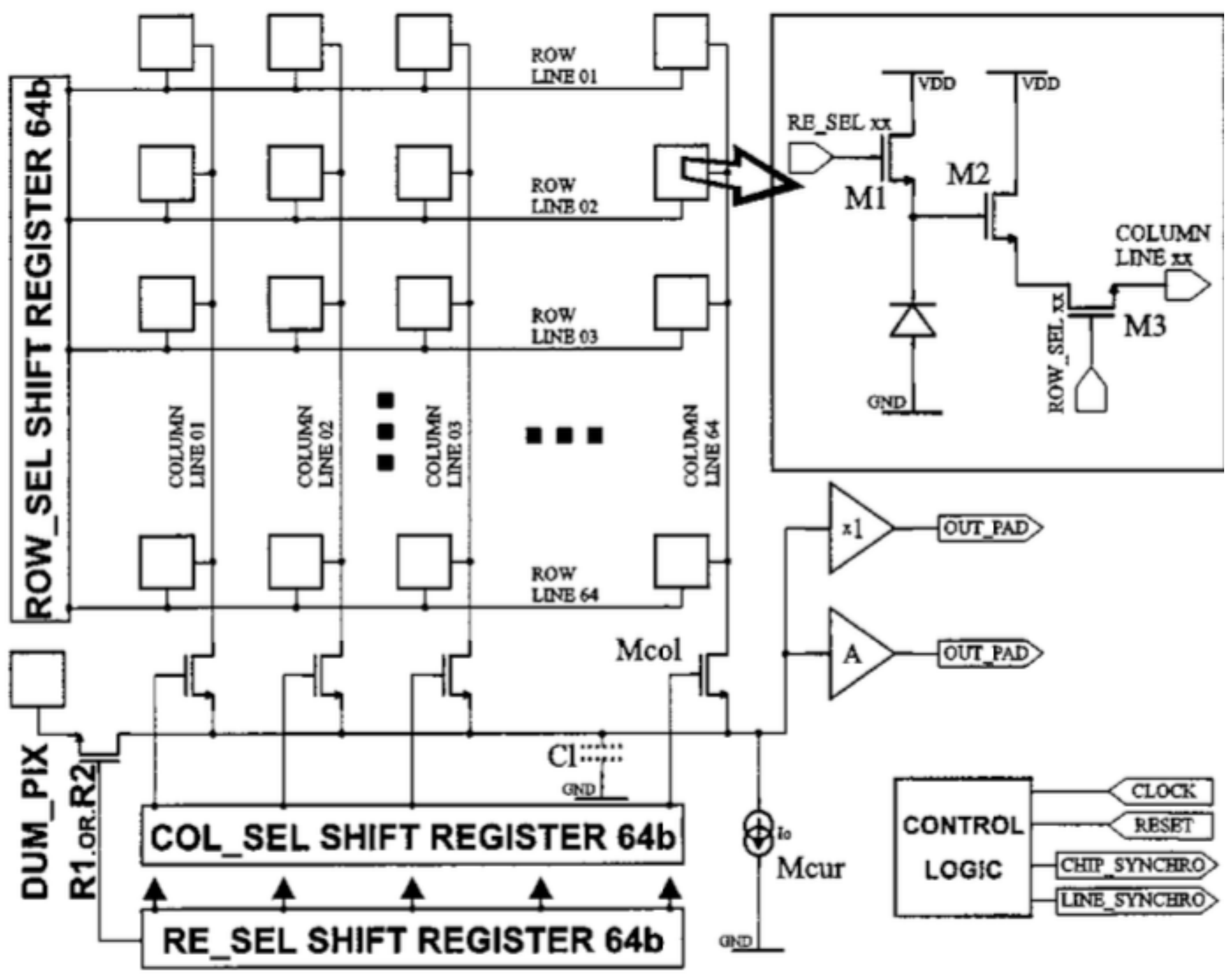
2. Do you like better the PACMAN [DATA DRIVEN read-out; e.g. token ring for the sake of simplicity]



or the camera [ROLLING shutter, possibly]?

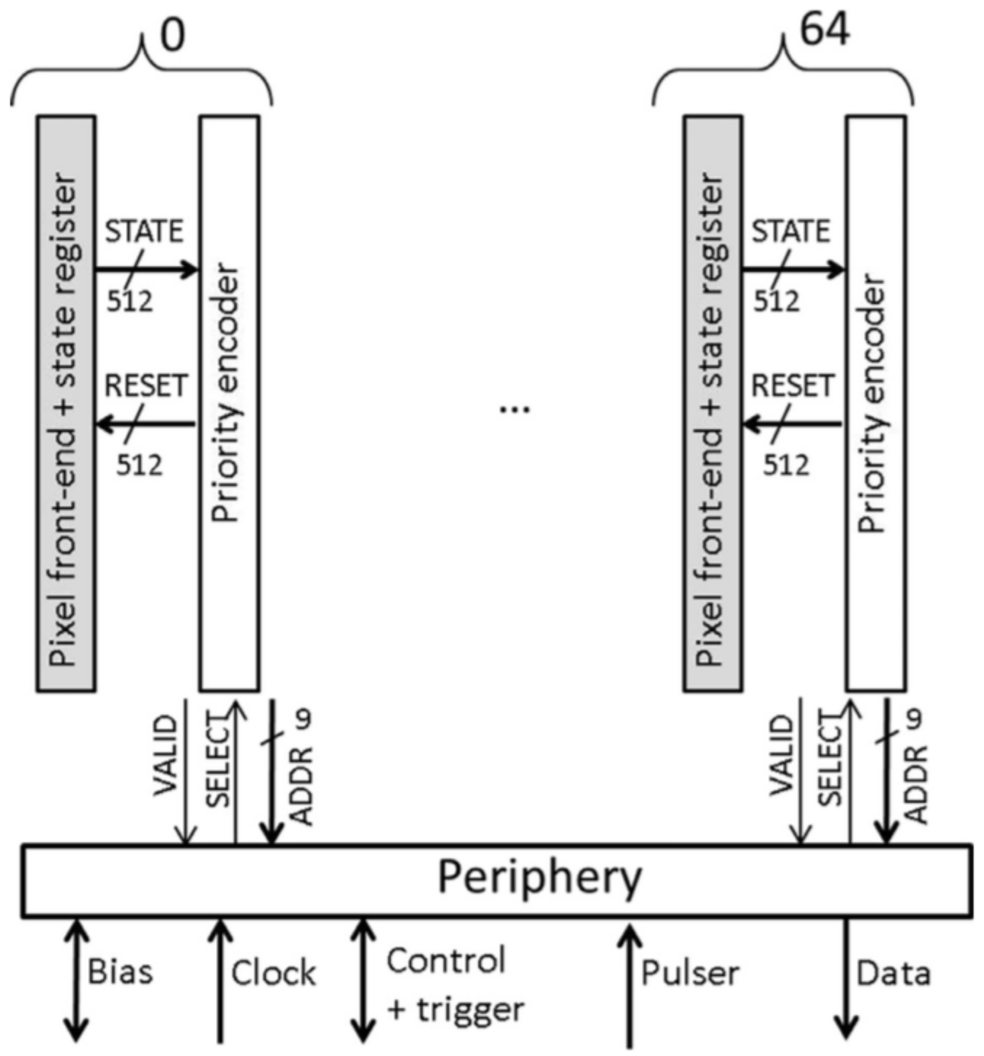


Rolling Shutter - MIMOSA-28



- 1 discriminator/column
  ⇢ analog info travels to the end-of-column logic
- the integration time is determined by the read-out (r.o.) time
- the r.o. time is independent from the pixel occupancy
- current power consumption at the level of 150 mW/cm²

On-pixel sparsification - ALPIDE



- 1 discriminator/pixel + 1bit memory cell
  ⇢ analog info locally processed
- the integration time is independent from read-out (r.o.) time
- the r.o. time is dependent from the pixel occupancy
- current power consumption at the level of 50 mW/cm²

-NIM A 765 (2014) 177 + A 785 (2015) 61
-pixel 2014 proceedings published on JINST
(doi: 10.1088/1748-0221/10/03/C03030)

4. CONCLUSIONS (1/3)

* The new technologies certainly offer unprecedented opportunities

* I believe the running conditions at the Z shall be carefully considered in designing the detector

* the real CHALLENGE, to me, will be designing an architecture providing the required data evacuation rate with the MINIMUM power dissipation, resulting by an optimisation of the ANALOG CELL, the digital architecture, the clock distribution

* **Having DESIGNERS on our side**, and considered the current level of activities , I see 3 options:

    - **be conservative&evolutionary**, starting by the ALPIDE design

    - **be smart**, exploit what we did in the past (e.g. the STm130nm design by the UNIPV-UNIBG teams) and what is being done (e.g. SEED (Sensor with Embedded Electronics Development - ITALY; MALTA lead by Bonn; ARCADIA, the INFN project just starting up)

    - **be brave**, start with something OUT-OF-THE-BOX

4. CONCLUSIONS (2/3)

vertex VENTURES

APPROACH INVESTMENTS TEAM VIEWPOINT CONTACT

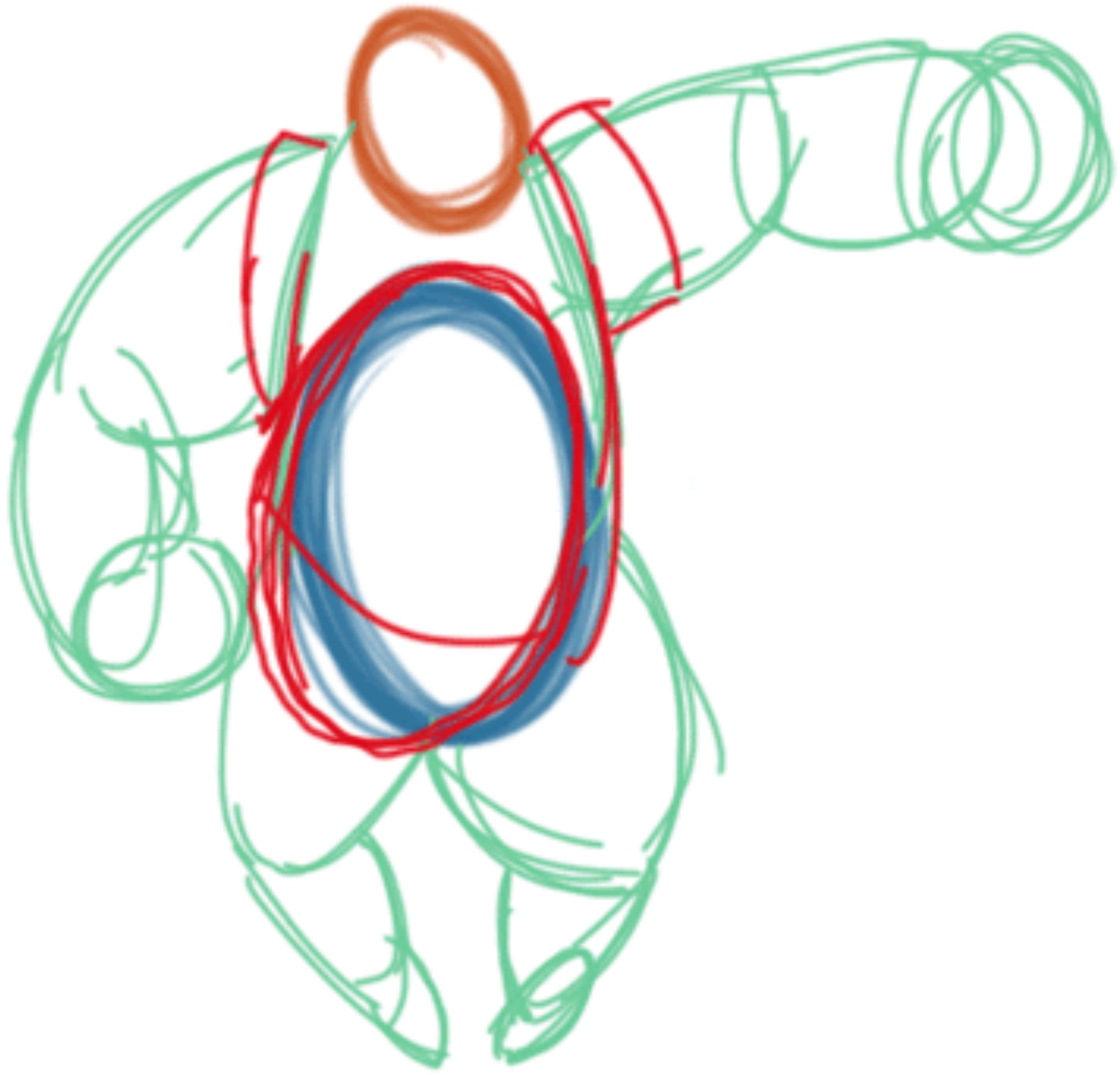
Game changers.

At Vertex, we continually push ourselves to improve, to strive for perfection; and we'll push you just as hard. That's because we see our investments not merely as a numbered percentage of ownership, but as a full-on engagement — a deeper and more regular involvement that compels you to think bigger than you are in order to make your idea successful.

Selected prior investments include angel investments and investments made at previous firms.

These are the companies.

4. CONCLUSIONS (3/3)



Let’s move on!

Thank you for listening!